

**P- Channel Enhancement Mode MOSFET**
**◆ DESCRIPTION**

The MT2561 is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

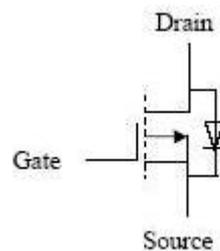
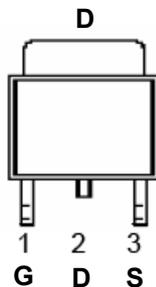
These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other Battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

**◆ FEATURES**

- -60V/-7A,  $R_{DS(ON)} = 90m\Omega @ V_{GS} = -10V$
- -60V/-6A,  $R_{DS(ON)} = 135m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely ultra low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252 package design

**◆ APPLICATIONS**

- POWER Management
- Portable Equipment
- DC/DC Converter
- Load Switch
- DSC

**◆ PIN CONFIGURATION**
**TO-252(Top Site)**


**P- Channel Enhancement Mode MOSFET**
**◆ ABSOLUTE MAXIMUM RATINGS**

 (T<sub>A</sub>=25°C Unless Otherwise Noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V <sub>DS</sub>	-60	V
Gate-Source Voltage		V <sub>GS</sub>	±20	V
Continuous Drain Current	T <sub>A</sub> = 25°C	I <sub>D</sub>	-12	A
	T <sub>A</sub> = 70°C		-10	
Pulsed Drain Current <sup>A</sup>		I <sub>DM</sub>	-30	A
Power Dissipation	T <sub>A</sub> = 25°C	P <sub>D</sub>	28	W
	T <sub>A</sub> = 70°C		18	
Operating junction temperature range		T <sub>J</sub>	- 55 to 150	°C
Storage temperature range		T <sub>STG</sub>	- 55 to 150	°C
Lead Temperature ( 1/16" form case for 10 Sec.)		T <sub>L</sub>	275	°C

Note A: Pulse width limited by maximum junction temperature.

Note B: Duty cycle ≤ 1%.

**◆ THERMAL RESISTANCE RATINGS**

Thermal Resistance	Symbol	Maximum	Unit
Junction-to-Case	R <sub>θJC</sub>	3	°C/W
Junction-to-Ambient	R <sub>θJA</sub>	75	°C/W

**◆ ORDERING INFORMATION**

Device	Package	Shipping
MT2561	TO-252	2,500 PCS / Tape & Reel

**P- Channel Enhancement Mode MOSFET**
**◆ ELECTRICAL CHARACTERISTICS**

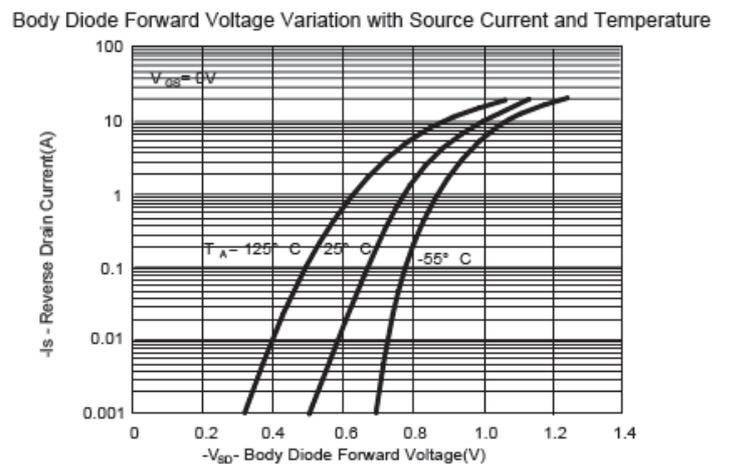
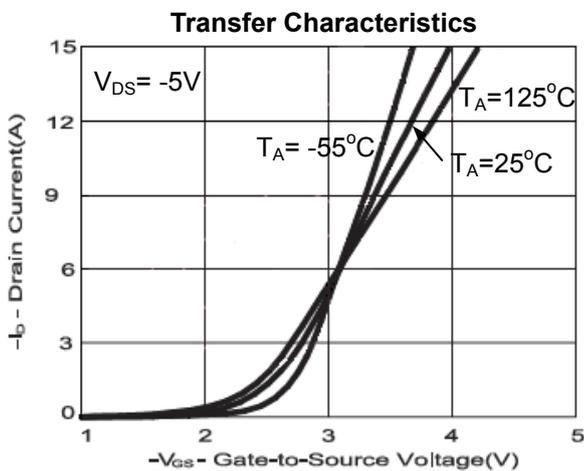
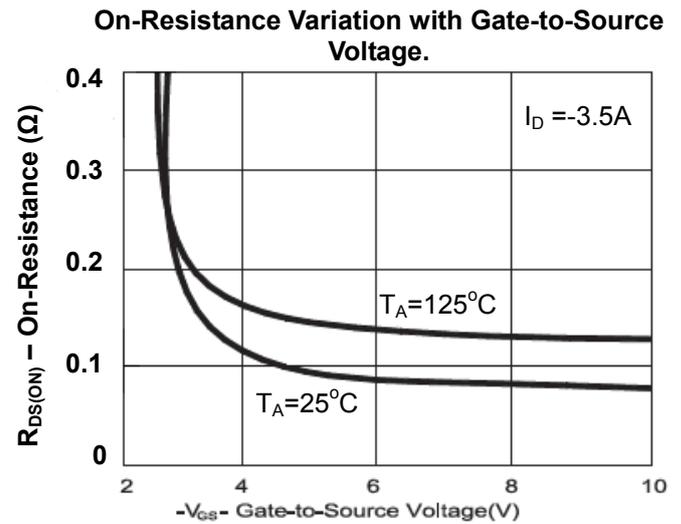
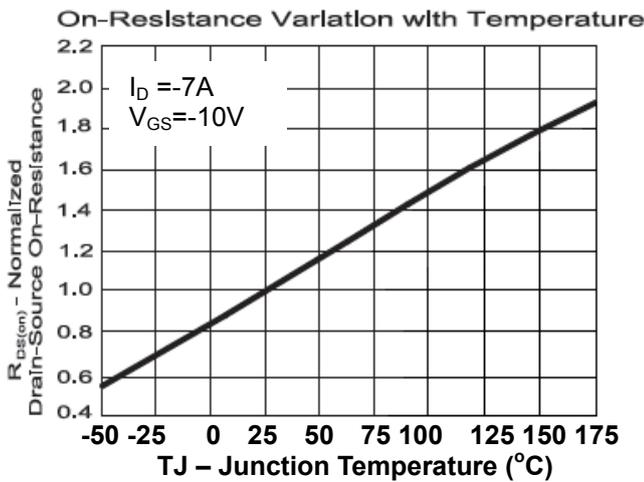
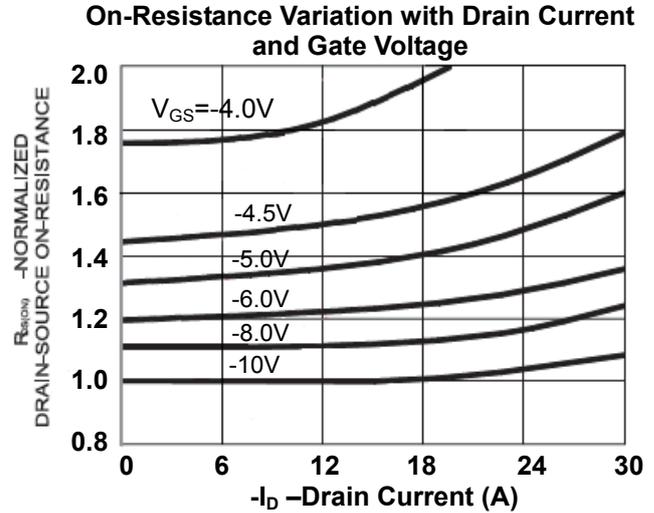
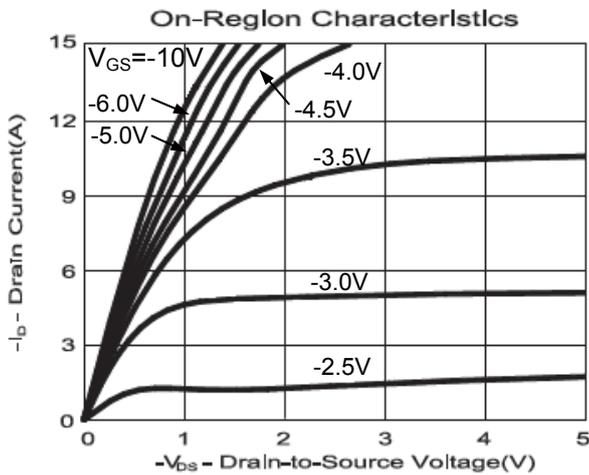
 (T<sub>A</sub>=25°C Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Parameters</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-60	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250μA	-1.0	-2.0	-3.0	V
Gate Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ± 20V	-	-	±250	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -48V, V <sub>GS</sub> = 0 V	-	-	-1	μA
		V <sub>DS</sub> = -44V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C	-	-	-10	
On-State Drain Current <sup>C</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = -5V, V <sub>GS</sub> = -10V	-32	-	-	A
Drain-Source On Resistance <sup>C</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -7A	-	100	135	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -6A	-	70	90	
Forward Trans conductance <sup>C</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -10V, I <sub>D</sub> = -7A	-	9	-	S
<b>Dynamic Parameters</b>						
Input Cap.	C <sub>iss</sub>	V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0V, f = 1MHz	-	760	-	pF
Output Cap.	C <sub>oss</sub>		-	90	-	
Reverse Transfer Cap.	C <sub>rss</sub>		-	40	-	
Total Gate Charge <sup>D</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 0.5V <sub>(BR)DSS</sub> , V <sub>GS</sub> = -10V, I <sub>D</sub> = -7A	-	15	-	nC
Gate-Source Charge <sup>D</sup>	Q <sub>gs</sub>		-	2.5	-	
Gate-Drain Charge <sup>D</sup>	Q <sub>gd</sub>		-	3.0	-	
Turn-On Time <sup>D</sup>	T <sub>D(ON)</sub>	V <sub>DS</sub> = -20V, I <sub>D</sub> = -1A, V <sub>GS</sub> = -10V, R <sub>G</sub> = 6Ω	-	7	14	nS
	t <sub>r</sub>		-	10	20	
Turn-Off Time <sup>D</sup>	T <sub>D(OFF)</sub>		-	19	34	
	t <sub>f</sub>		-	12	22	
<b>Source-Drain Diode Ratings And Characteristics</b>						
Continuous Current	I <sub>S</sub>		-	-	-1.3	A
Pulsed Current <sup>E</sup>	I <sub>SM</sub>		-	-	-2.6	
Forward Voltage <sup>C</sup>	V <sub>SD</sub>	I <sub>F</sub> = I <sub>S</sub> , V <sub>GS</sub> = 0V	-	-	-1	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -7A, dI/dt = 100A/μS	-	15.5	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	7.9	-	nC

Note C: Pulse test: Pulse width ≤ 300μsec, Duty Cycle ≤ 2%

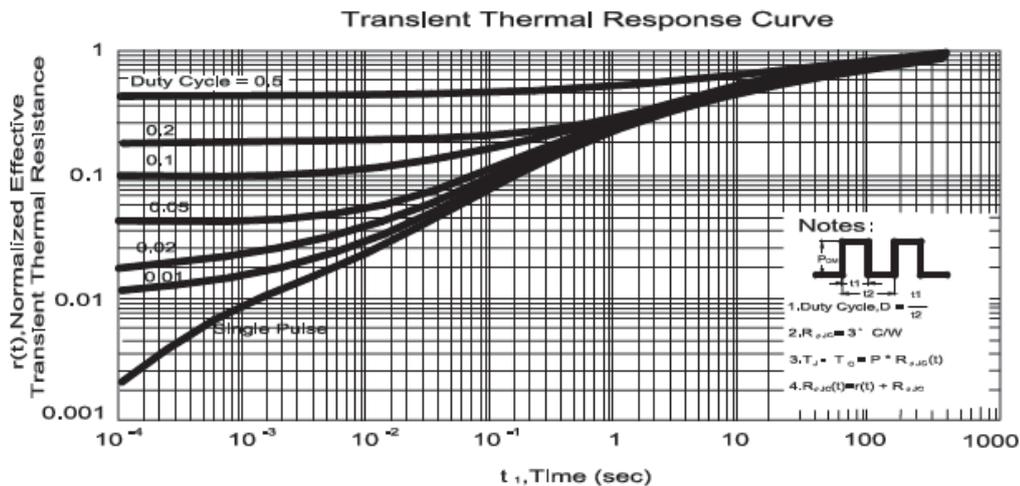
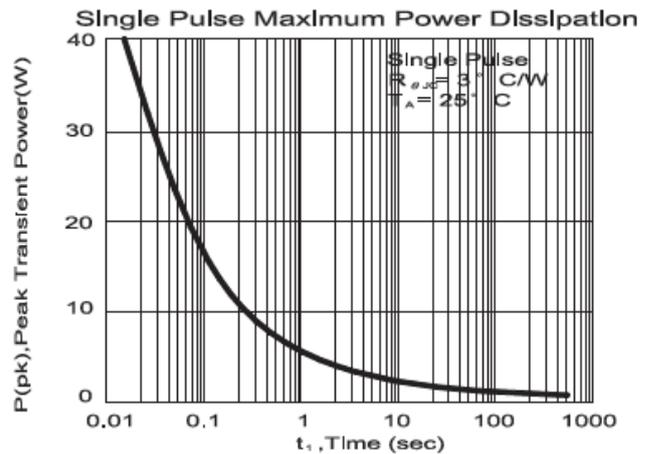
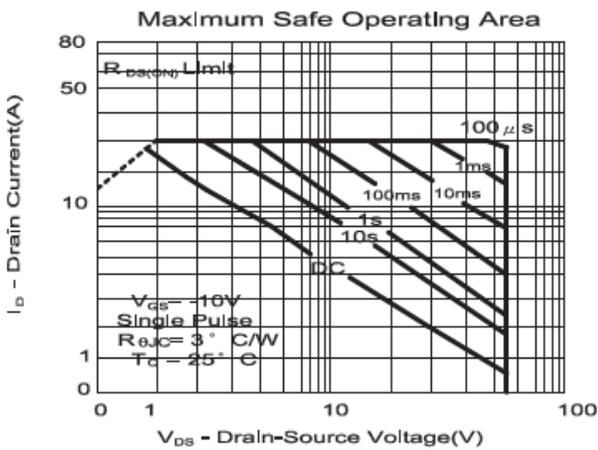
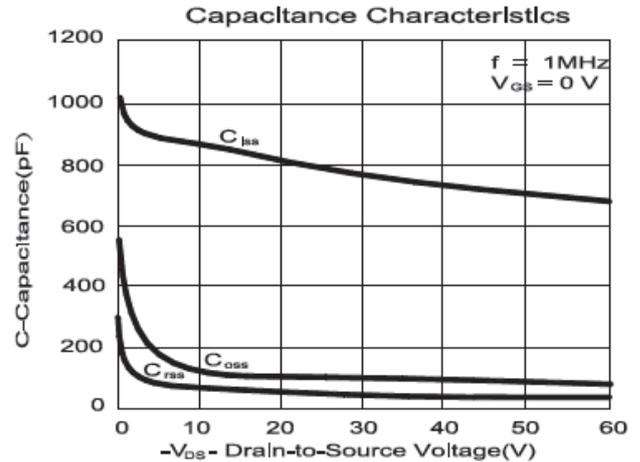
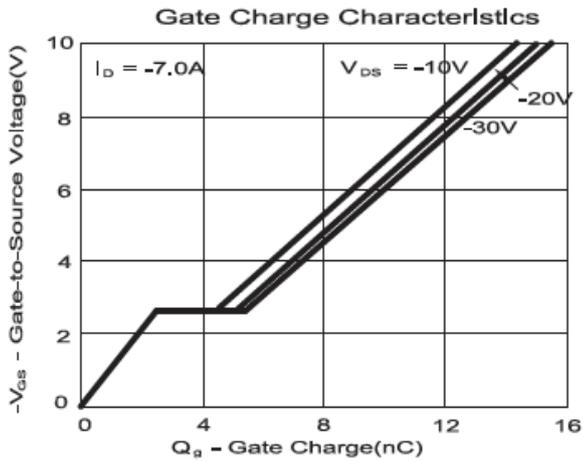
Note D: Independent of operating temperature.

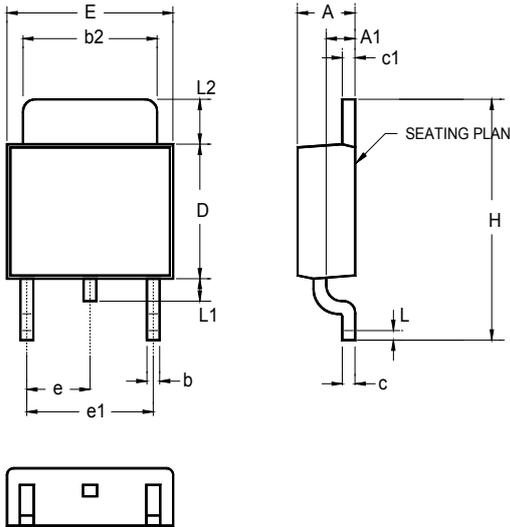
Note E: Pulse width limited by maximum junction temperature.

**P- Channel Enhancement Mode MOSFET**
**◆ TYPICAL CHARACTERISTICS (25°C Unless Noted)**


**P- Channel Enhancement Mode MOSFET**
**◆ TYPICAL CHARACTERISTICS**

(25°C Unless Noted)



**P- Channel Enhancement Mode MOSFET**
**◆ PHYSICAL DIMENSIONS**
**3-Pin Surface Mount TO-252 (B)**


	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.086	-	0.094	2.18	-	2.39
A1	0.040	-	0.050	1.02	-	1.27
b	-	0.024	-	-	0.61	-
b2	0.205	-	0.215	5.21	-	5.46
c	0.018	-	0.023	0.46	-	0.58
c1	0.018	-	0.023	0.46	-	0.58
D	0.210	-	0.220	5.33	-	5.59
E	0.250	-	0.265	6.35	-	6.73
e	0.090 BSC			2.29 BSC		
e1	0.180 BSC			4.58 BSC		
H	0.370	-	0.410	9.40	-	10.41
L	0.020	-	-	0.51	-	-
L1	0.025	-	0.040	0.64	-	1.02
L2	0.060	-	0.080	1.52	-	2.03