P- Channel Enhancement Mode MOSFET

◆ DESCRIPTION

The MT2501 is the P-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other Battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

◆ FEATURES

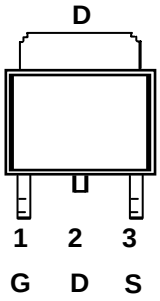
- -100V/-10A, $R_{DS(ON)}$ =205mΩ @ V_{GS} = -10V
- -100V/-10A, $R_{DS(ON)}$ =225mΩ @ V_{GS} = -7V
- Super high density cell design for extremely ultra low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252 package design

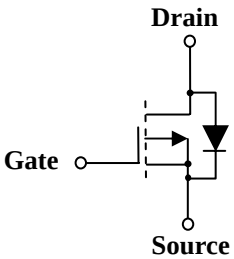
◆ APPLICATIONS

- POWER Management
- Portable Equipment
- DC/DC Converter
- Load Switch
- DSC

◆ PIN CONFIGURATION

TO-252(Top Site)





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◆ ABSOLUTE MAXIMUM RATINGS

(T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	-100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A = 25℃	I_D	-10	A
	T_A = 100℃		-7	
Pulsed Drain Current [A]		I_{DM}	-40	A
Avalanche Current		I_{AS}	-12	A
Avalanche Energy(L=0.1mH, I_D =-12A,R_G=25Ω)		E_{AS}	7.2	mJ
Repetitive Avalanche Energy [B](L=0.05mH)		E_{AR}	3.6	
Power Dissipation	T_A = 25℃	P_D	35	W
	T_A = 100℃		15	
Operating junction temperature range		T_J	- 55 to 175	°C
Storage temperature range		T_{STG}	- 55 to 175	°C

Note [A]: Pulse width limited by maximum junction temperature.
[B]: Duty cycle ≦ 1%.

◆ THERMAL RESISTANCE RATINGS

Thermal Resistance	Symbol	Maximum	Unit
Junction-to-Case	$R_{\theta JC}$	4.3	°C/W
Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

◆ ORDERING INFORMATION

Device	Package	Shipping
MT2501	TO-252	2,500 PCS / Tape & Reel

◆ ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -250μA	-1	-2	-3	V
Gate Current	I_{GSS}	V_{DS} = 0V, V_{GS} = ± 20V	-	-	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80V, V_{GS} = 0 V	-	-	-1	μA
		V_{DS} =-70V, V_{GS} = 0V, T_J = 125°C	-	-	-25	
On-State Drain Current [A]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-10	-	-	A
Drain-Source On Resistance [A]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -10A	-	182	205	mΩ
		V_{GS} = -7 V, I_D = -10A	-	190	225	
Forward Trans conductance [A]	g_{fs}	V_{DS} = -5V, I_D = -10A	-	7	-	S
Dynamic Parameters						
Input Cap.	C_{iss}	V_{DS} = -25V, V_{GS} = 0V, f = 1MHz	-	2018	-	pF
Output Cap.	C_{oss}		-	500	-	
Reverse Transfer Cap.	C_{rss}		-	352	-	
Gate Resistance	Rg	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz	-	4.5	-	Ω
Total Gate Charge [A,B]	Q_g	V_{DS} = -80V, V_{GS} =- 10V, I_D = -10A	-	31	-	nC
Gate-Source Charge [A,B]	Q_{gs}		-	6.3	-	
Gate-Drain Charge [A,B]	Q_{gd}		-	4.5	-	
Turn-On Time [A,B]	$T_{D(ON)}$	V_{DS} = -10V, I_D = -1A, V_{Gs} = -10V, R_{GS} = 6Ω	-	12	-	nS
Rise Time [A,B]	t_r		-	55	-	
Turn-Off Time [A,B]	$T_{D(OFF)}$		-	40	-	
Fail Time [A,B]	t_f		-	40	-	
Source-Drain Diode Ratings And Characteristics						
Continuous Current	I_S		-	-	-10	A
Pulsed Current [C]	I_{SM}		-	-	-40	
Forward Voltage [A]	V_{SD}	I_F = I_S , V_{GS} = 0V	-	-	1.3	V
Reverse Recovery Time	t_{rr}	I_F = -5A , dI_F/dt=100A/μS	-	70	-	nS
Reverse Recovery Charge	Q_{rr}		-	420	-	nC

Note [A]: Pulse test: Pulse width ≤ 300μsec, Duty Cycle ≤ 2%

[B]: Independent of operating temperature

[C]: Pulse width limited by maximum junction temperature.

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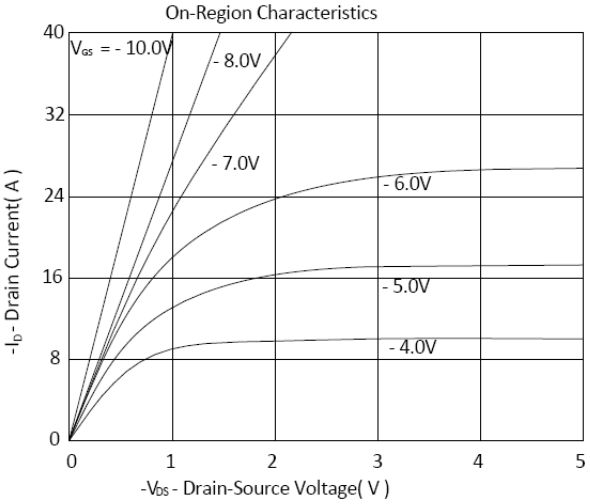
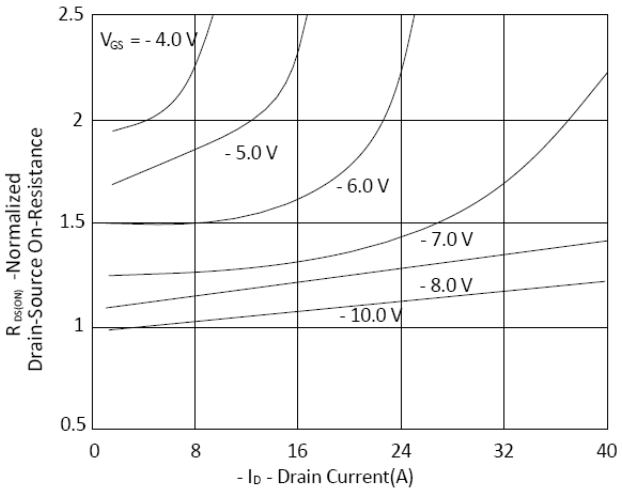
◆ TYPICAL CHARACTERICTICS

(25℃ Unless Noted)

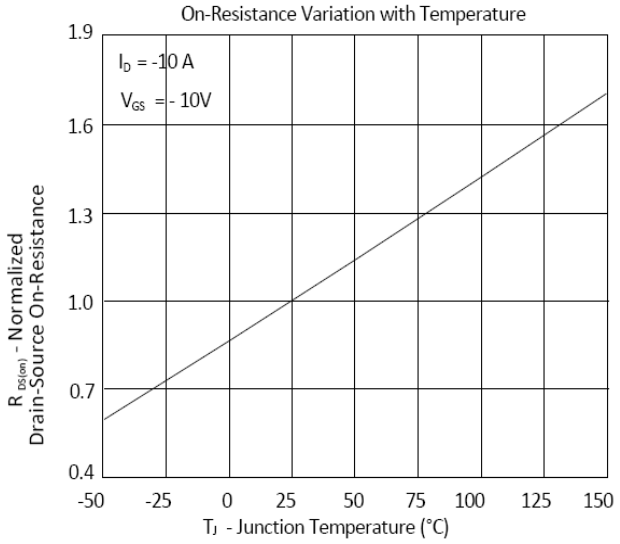
On-Region Characteristics



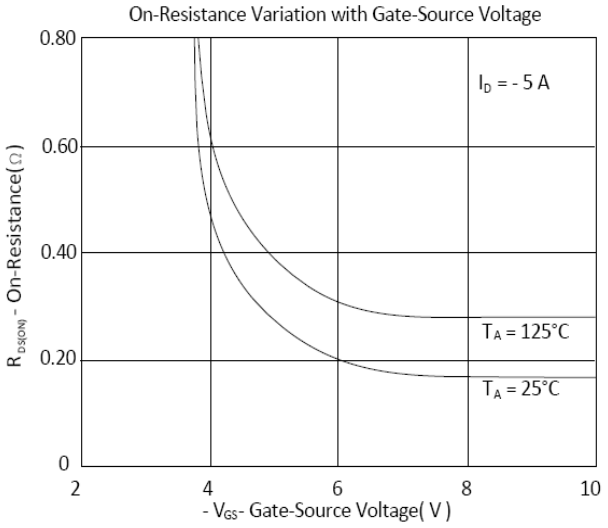
On-Resistance Variation with Drain Current and Gate Voltage



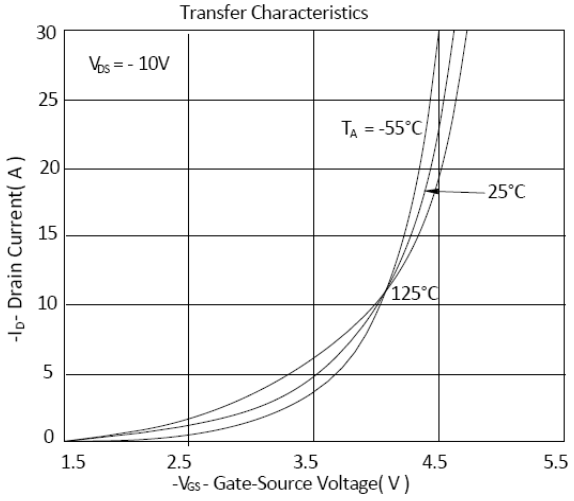
On-Resistance Variation with Temperature



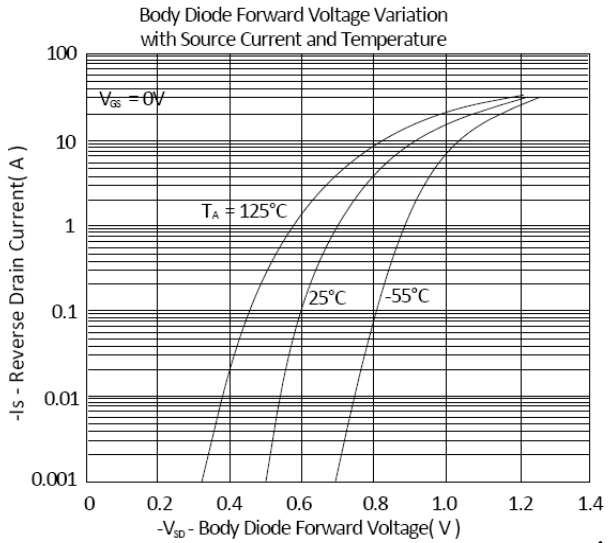
On-Resistance Variation with Gate-Source Voltage



Transfer Characteristics



Body Diode Forward Voltage Variation with Source Current and Temperature

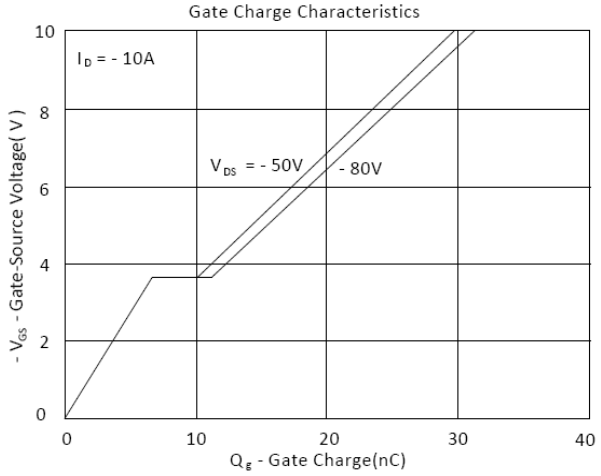


P- Channel Enhancement Mode MOSFET

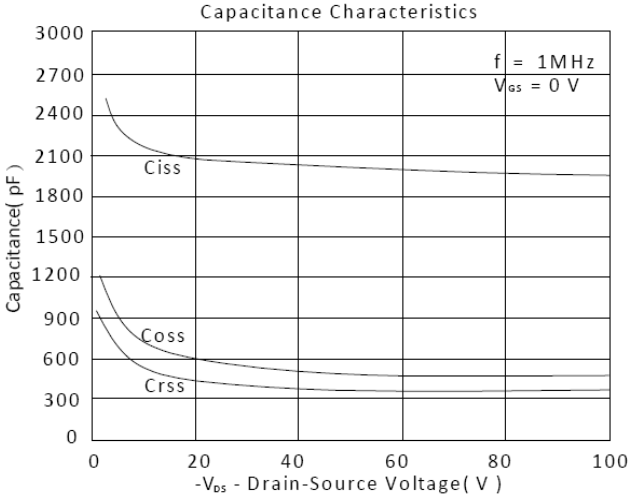
◆ TYPICAL CHARACTERICTICS

(25℃ Unless Noted)

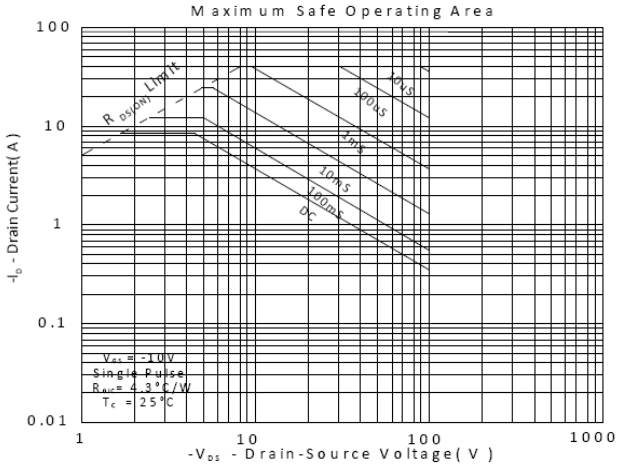
Gate Charge Characteristics



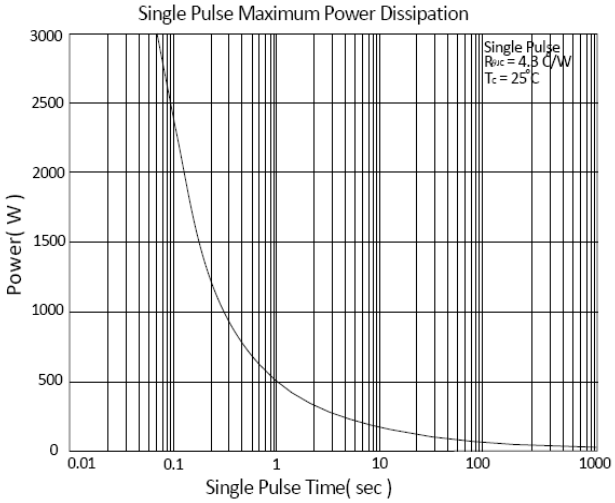
Capacitance Characteristics



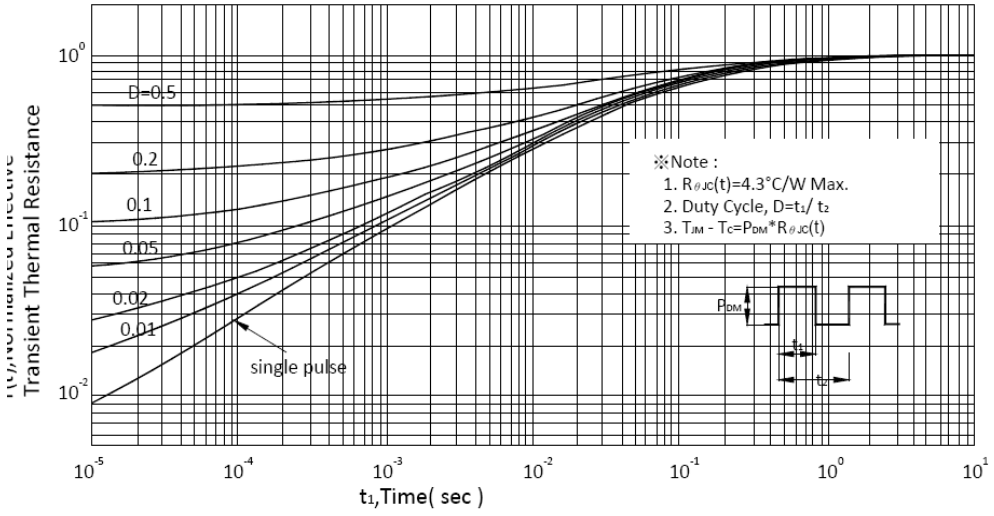
Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation

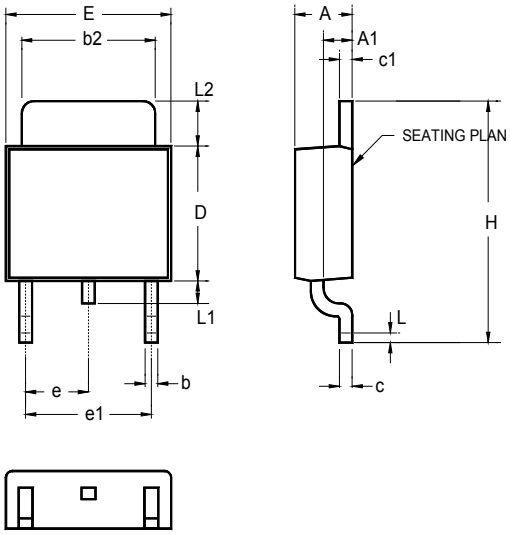


Transient Thermal Response Curve



◆ PHYSICAL DIMENSIONS

3-Pin Surface Mount TO-252 (B)



	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.086	-	0.094	2.18	-	2.39
A1	0.040	-	0.050	1.02	-	1.27
b	-	0.024	-	-	0.61	-
b2	0.205	-	0.215	5.21	-	5.46
c	0.018	-	0.023	0.46	-	0.58
c1	0.018	-	0.023	0.46	-	0.58
D	0.210	-	0.220	5.33	-	5.59
E	0.250	-	0.265	6.35	-	6.73
e	0.090 BSC			2.29 BSC		
e1	0.180 BSC			4.58 BSC		
H	0.370	-	0.410	9.40	-	10.41
L	0.020	-	-	0.51	-	-
L1	0.025	-	0.040	0.64	-	1.02
L2	0.060	-	0.080	1.52	-	2.03