◆ DESCRIPTION

The MT7402 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

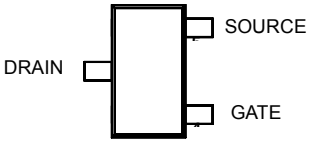
◆ FEATURES

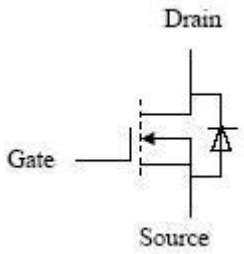
- 20V/4.0A,RDS(ON)=65mΩ@VGS=4.5V
- 20V/3.4A,RDS(ON)=80mΩ@VGS=2.5V
- 20V/2.8A,RDS(ON)=95mΩ@VGS=1.8V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- SOT-323 (SC–70-3L) package design

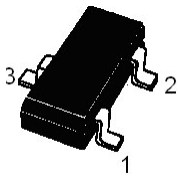
◆ APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

◆ PIN CONFIGURATION







◆ ABSOLUTE MAXIMUM RATINGS (Ta=25℃ Unless Otherwise Noted)

SYMBOL	PARAMETER		MAXIMUM	UNITS
V_{DS}	Drain-Source Voltage		20	V
V_{GS}	Gate-Source Voltage		±12	V
I_D	Continuous Drain Current	Tc= 25℃	2.4	A
		Tc= 70℃	1.7	
I_{DM}	Pulsed Drain Current		6	A
I_S	Continuous Source Current (Diode Conduction)		1.6	A
P_D	Power Dissipation	Tc= 25℃	1.19	W
		Tc= 70℃	0.76	
T_J	Operating junction temperature range		-55 to 150	°C
T_{STG}	Storage temperature range		- 55 to 150	°C

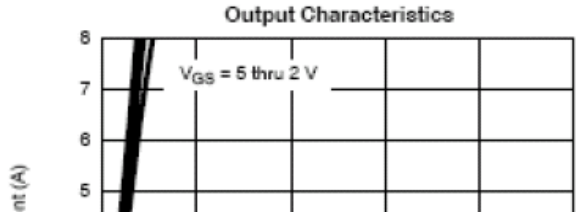
◆ THERMAL RESISTANCE RATINGS

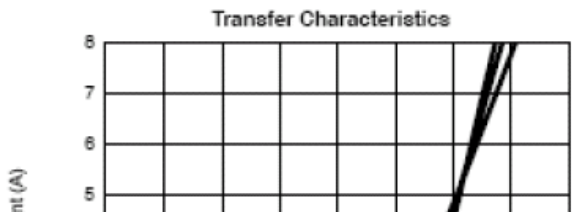
Thermal Resistance	Symbol	Maximum	UNIT
Junction-to-Ambient	$R_{\theta JA}$	105	°C/W

◆ ELECTRICAL CHARACTERISTICS: (Ta= 25℃ Unless Otherwise Noted)

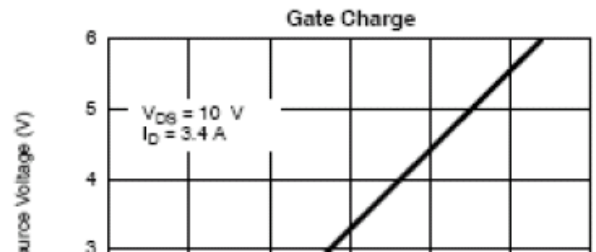
SYMBOL	PARAMETER	TEST CONDITIONs	MIN	TYP	MAX	UNITS
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D=250μA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D=250μA	0.35		0.85	V
I_{GSS}	Gate Leakage current	V_{DS} = 0V, V_{GS} = ±12 V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20V, V_{GS} = 0 V			1	μA
		V_{DS} = 20V, V_{GS} = 0 V, T_J=55°C			5	
$I_{D(ON)}$	On-State Drain Current	V_{DS}≦5V,V_{GS}=4.5V	6			A
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS} = 4.5V, I_D=4.0A		0.060	0.065	Ω
		V_{GS}= 2.5V, I_D=3.4A		0.067	0.080	
		V_{GS}= 1.8V, I_D=2.8A		0.076	0.095	
g_{fs}	Forward Transconductance	V_{DS}=5V,I_D=-3.6A		10		S
V_{SD}	Diode Forward Voltage	I_S=1.6A,V_{GS}=0V		0.8	1.2	V
Dynamic Parameters						
C_{iss}	Input Cap.	V_{DS}=6V,V_{GS}=0V F=1MHz		485		pF
C_{oss}	Output Cap.			85		
C_{rss}	Reverse Transfer Cap.			40		
Q_g	Total Gate Charge	V_{DS}=6V,V_{GS}=4.5V I_D=2.8A		4.8	8	nC
Q_{gs}	Gate-Source Charge			1.0		
Q_{gd}	Gate-Drain Charge			1.0		
$t_{d(on)}$	Turn-On Time	V_{DD}=6V,R_L=6Ω I_D=1.0A, V_{GEN}=4.5V ,R_G=6Ω		8	14	ns
t_r				12	18	
$T_{d(off)}$	Turn-Off Time			30	35	
t_f				12	16	

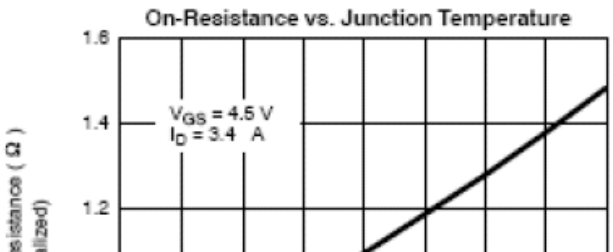
◆ TYPICAL CHARACTERISTICS



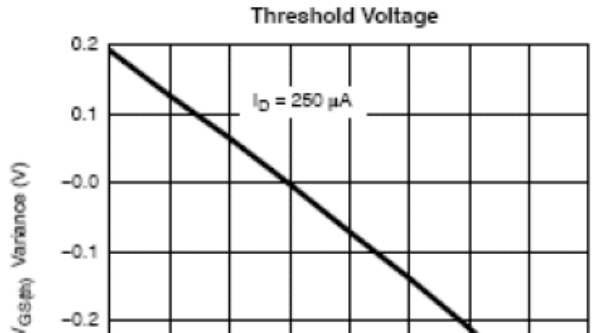


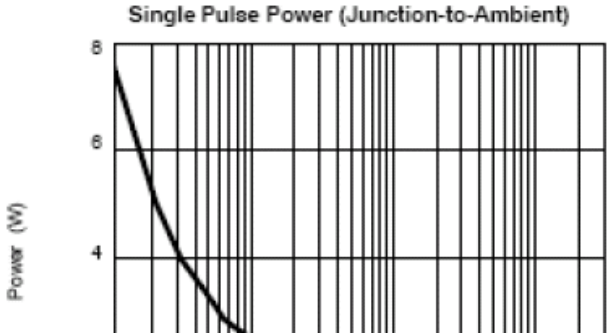
◆ TYPICAL CHARACTERISTICS





◆ TYPICAL CHARACTERISTICS





◆ SOT-323 PACKAGE OUTLINE

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