

◆ DESCRIPTION

The MT7400 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

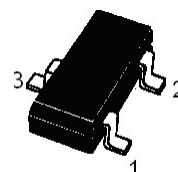
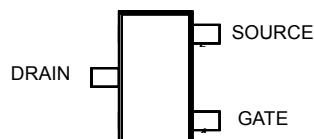
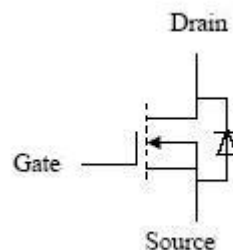
These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

◆ FEATURES

- 30V/2.8A, RDS(ON)= 77mΩ@VGS=10V
- 30V/2.3A, RDS(ON)= 85mΩ@VGS=4.5V
- 30V/1.5A, RDS(ON)= 110mΩ@VGS=2.5V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- SOT-323 (SC-70-3L) package design

◆ APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch DSC
- LCD Display inverter

◆ PIN CONFIGURATION


N-Channel Enhancement Mode MOSFET
◆ ABSOLUTE MAXIMUM RATINGS (Ta=25°C Unless Otherwise Noted)

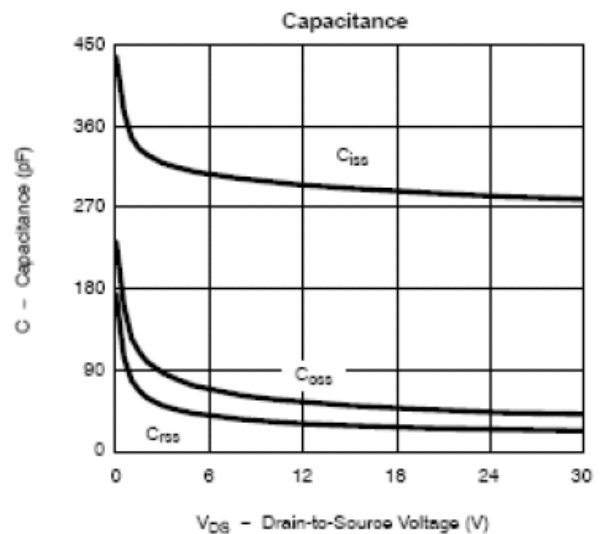
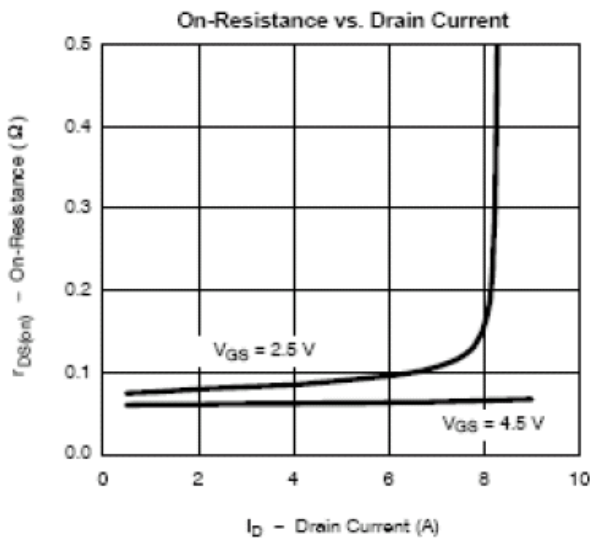
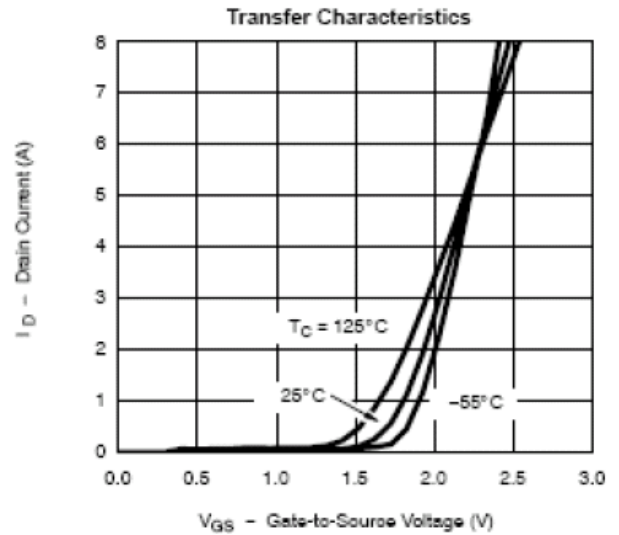
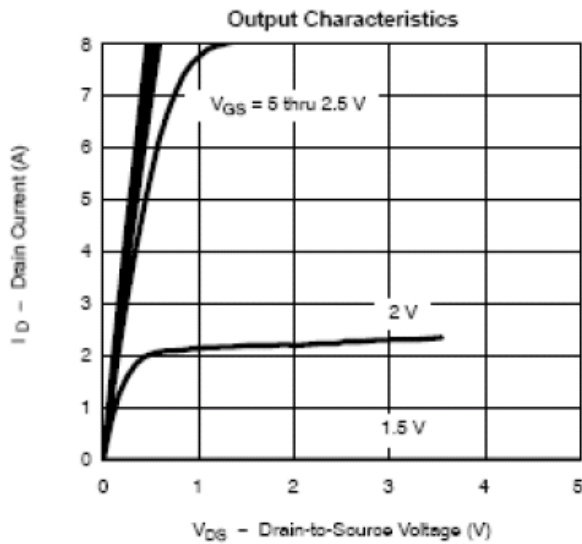
SYMBOL	PARAMETER	MAXIMUM	UNITS
V _{DS}	Drain-Source Voltage	30	V
V _{GS}	Gate-Source Voltage	±12	V
I _D	Continuous Drain Current	T _c = 25°C	2.8
		T _c = 70°C	2.3
I _{DM}	Pulsed Drain Current	10	A
I _S	Continuous Source Current (Diode Conduction)	1.25	A
P _D	Power Dissipation	T _c = 25°C	1.25
		T _c = 70°C	0.8
T _J	Operating junction temperature range	150	°C
T _{STG}	Storage temperature range	- 55 to 150	°C

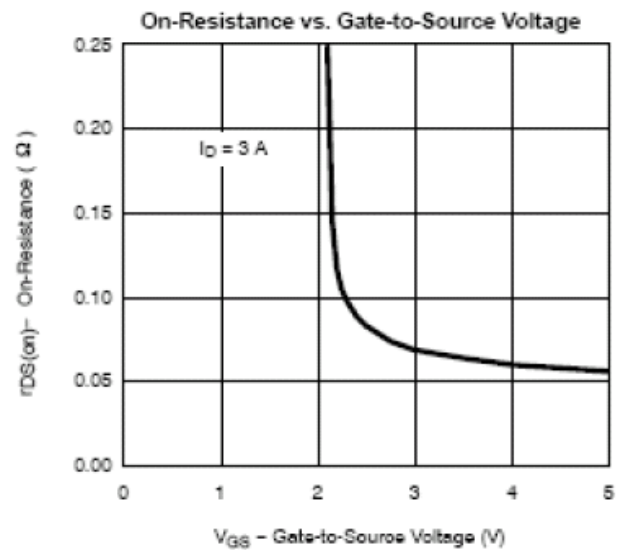
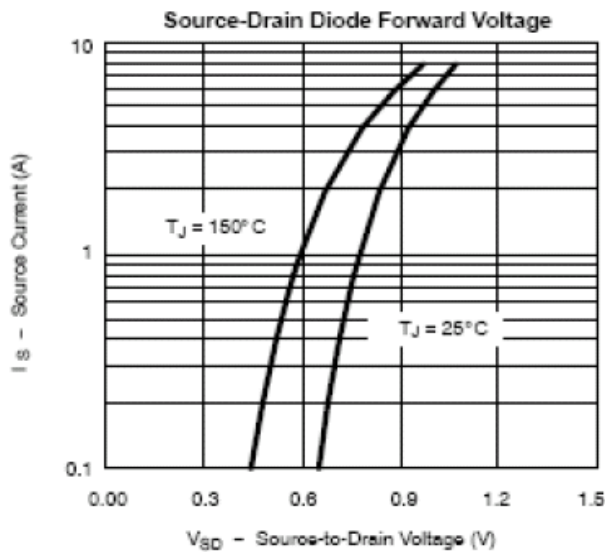
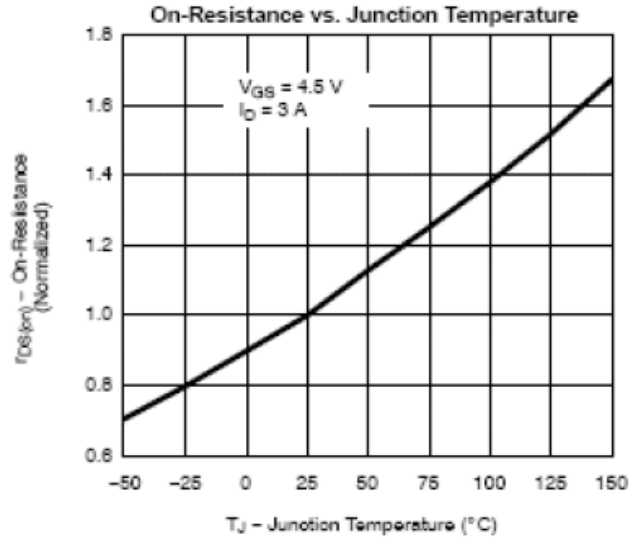
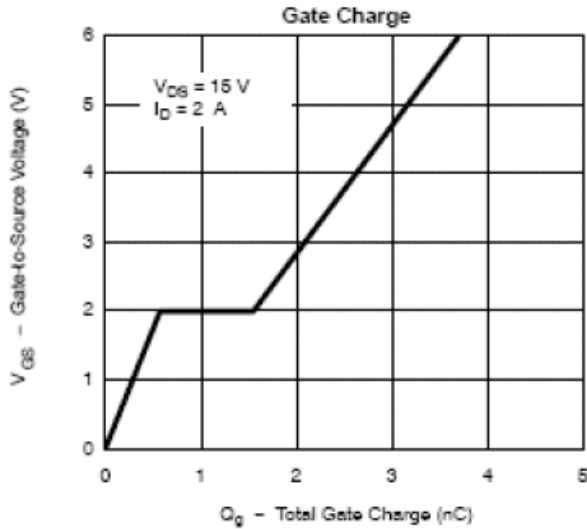
◆ THERMAL RESISTANCE RATINGS

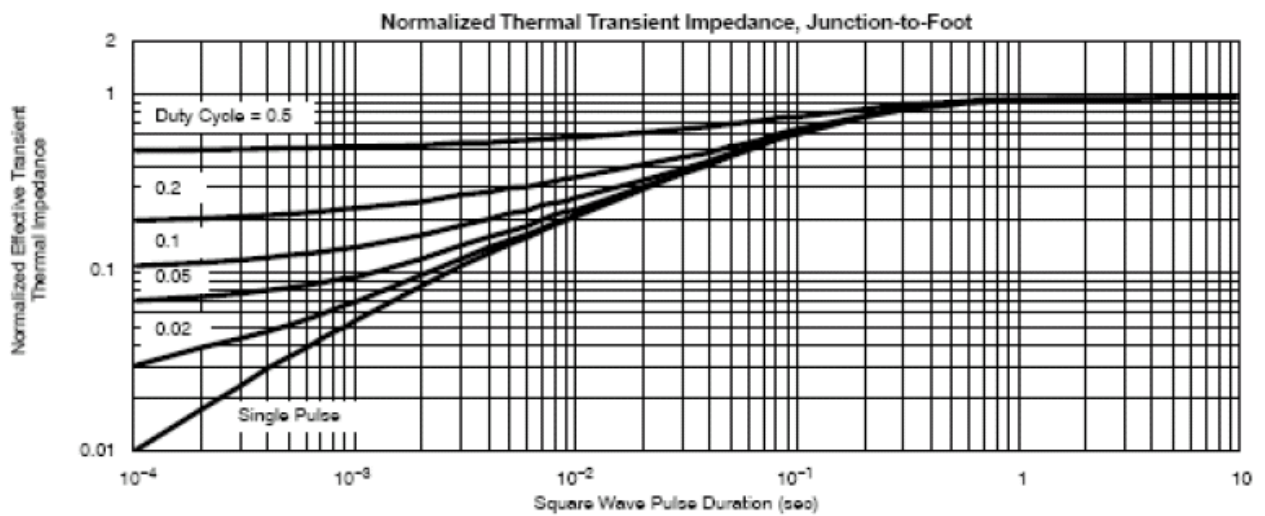
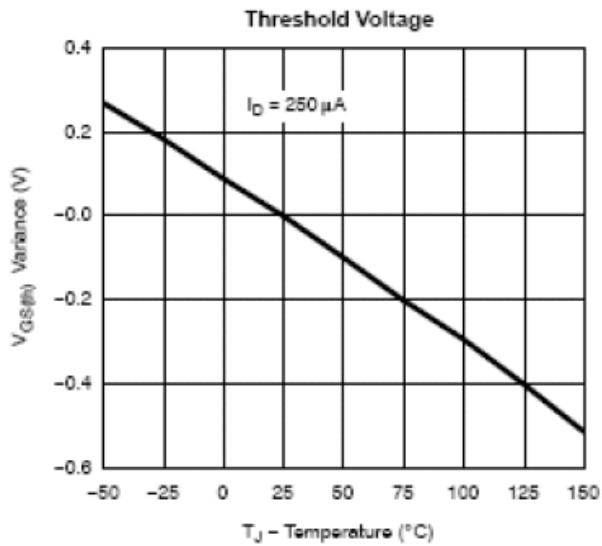
Thermal Resistance	Symbol	Maximum	UNIT
Junction-to-Ambient	R _{θJA}	100	°C/W

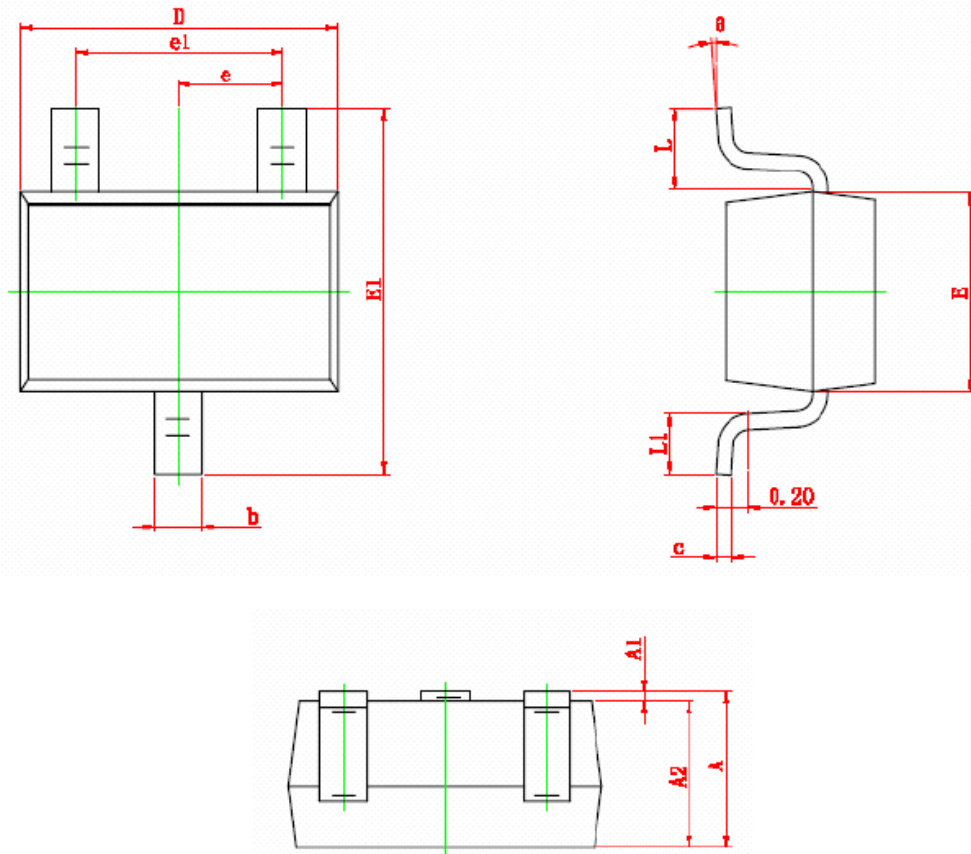
N-Channel Enhancement Mode MOSFET
◆ ELECTRICAL CHARACTERISTICS: (Ta= 25°C Unless Otherwise Noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.8		1.6	V
I_{GSS}	Gate Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 12V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24V, V_{GS} = 0V$			1	μA
		$V_{DS} = 24V, V_{GS} = 0V, T_J = 55^\circ C$			10	
$I_{D(ON)}$	On-State Drain Current	$V_{DS} \geq 4.5V, V_{GS} = 10V$	6			A
		$V_{DS} \geq 4.5V, V_{GS} = 4.5V$	4			A
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS} = 10V, I_D = 2.8A$		0.062	0.077	Ω
		$V_{GS} = 4.5V, I_D = 2.3A$		0.070	0.085	
		$V_{GS} = 2.5V, I_D = 1.5A$		0.095	0.110	
g_{fs}	Forward Transconductance	$V_{DS} = 4.5V, I_D = 2.8A$		4.6		S
V_{SD}	Diode Forward Voltage	$I_S = 1.25A, V_{GS} = 0V$		0.82	1.2	V
Dynamic Parameters						
C_{iss}	Input Cap.	$V_{DS} = 15V, V_{GS} = 0V, F = 1MHz$		350		μF
C_{oss}	Output Cap.			55		
C_{rss}	Reverse Transfer Cap.			41		
Q_g	Total Gate Charge	$V_{DS} = 15V, V_{GS} = 4.5V, I_D = 2.0A$		4.2	6	nC
Q_{gs}	Gate-Source Charge			0.6		
Q_{gd}	Gate-Drain Charge			1.5		
$t_{d(on)}$	Turn-On Time	$V_{DD} = 15V, R_L = 10\Omega, V_{GEN} = 10V, R_G = 3\Omega$		2.5		ns
t_r				2.5		
$T_{d(off)}$	Turn-Off Time			20		
t_f				4		

◆ TYPICAL CHARACTERISTICS


◆ TYPICAL CHARACTERISTICS


◆ TYPICAL CHARACTERISTICS


◆ SOT-323 PACKAGE OUTLINE


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.200	0.400	0.008	0.016
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0.055
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°