P-Channel Enhancement Mode MOSFET

◆ DESCRIPTION

The MT3413 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other batter powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package

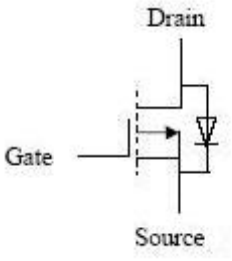
◆ FEATURES

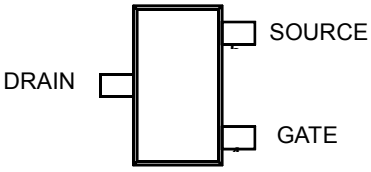
- -20V/-3.4A, $R_{DS(ON)}$ = 95 mΩ @ V_{GS} = -4.5V
- -20V/-2.6A, $R_{DS(ON)}$ = 120 mΩ @ V_{GS} = -2.5V
- -20V/-1A, $R_{DS(ON)}$ = 145 mΩ @ V_{GS} = -1.8V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

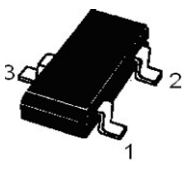
◆ APPLICATIONS

- POWER Management in Note
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC

◆ PIN CONFIGURATION







P-Channel Enhancement Mode MOSFET

◆ ABSOLUTE MAXIMUM RATINGS

(T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current	T_A = 25℃	I_D	-3.4	A
	T_A = 70℃		-2.4	
Pulsed Drain Current		I_{DM}	-15	A
Continuous Source Current (Diode Conduction)		I_S	-2	A
Power Dissipation	T_A = 25℃	P_D	1.4	W
	T_A = 70℃		0.9	
Operating junction temperature range		T_J	150	°C
Storage temperature range		T_{STG}	- 55 to 150	°C

◆ THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Unit
Junction-to-Ambient	$R_{\theta JA}$	100	°C/W

◆ ORDERING INFORMATION

Device	Package	Shipping
MT3413	SOT-23	3000 PCS / Tape & Reel

◆ ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless Otherwise Noted)

Static Parameters						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = $V_{DS,}$ I_D = 250μA	0.4	-	0.8	V
Gate Leakage Current	I_{GSS}	V_{DS} = 0V, V_{GS} = ± 12 V	-	-	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -20V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} =-20V, V_{GS} = 0V, T_J = 55 ℃	-	-	5	
Forward Trans conductance	g_{fs}	V_{DS} = -5V, ID = -3.4A	-	7	-	S
On-State Drain Current	$I_{D(ON)}$	V_{DS} ≤ -5V, V_{GS} = -4.5V	-15	-	-	A
Drain-Source On Resistance	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -3.4A	-	80	95	mΩ
		V_{GS} = -2.5V, I_D =- 2.6A	-	105	120	
		V_{GS} = -1.8V, I_D = -1.0A	-	130	145	
Diode Forward Voltage	V_{SD}	I_S = -1.0A, V_{GS} = 0V	-	0.75	-1.0	V
Dynamic Parameters						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Input Cap.	C_{iss}	V_{DS} = -10V, V_{GS} = 0V, F = 1MHz	-	540	-	pF
Output Cap.	C_{oss}		-	72	-	
Reverse Transfer Cap.	C_{rss}		-	49	-	
Total Gate Charge	Q_g	V_{DS} = -10V, V_{GS} = -4.5V, I_D = -1.0A	-	6.1	-	nC
Gate-Source Charge	Q_{gs}		-	0.6	-	
Gate-Drain Charge	Q_{gd}		-	1.6	-	
Turn-On Time	$T_{D(ON)}$	V_{DS} = -10V, R_L = 3.3Ω, V_{GEN} = -4.5V, R_G = 3Ω	-	10	-	nS
	t_r		-	12	-	
Turn-Off Time	$T_{D(OFF)}$		-	44	-	
	t_f		-	22	60	

◆ TYPICAL CHARACTERICTICS

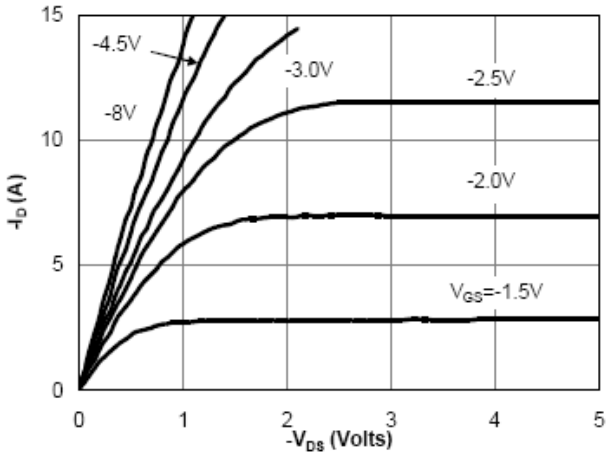


Fig 1: On-Region Characteristics

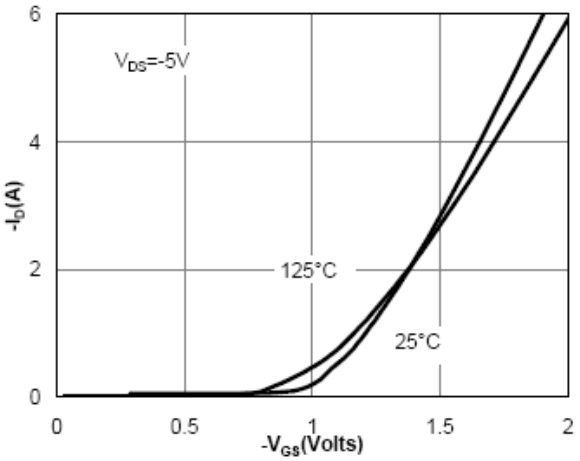


Figure 2: Transfer Characteristics

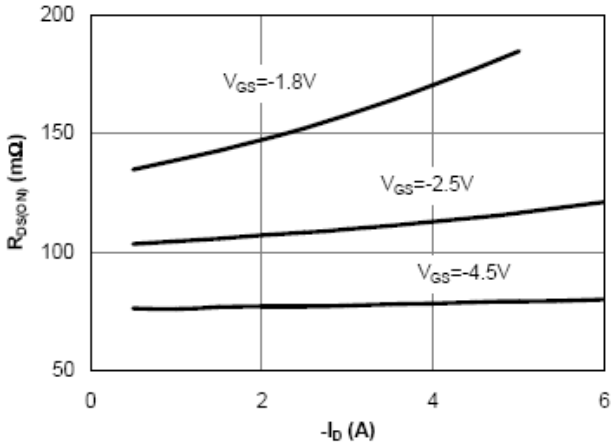


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

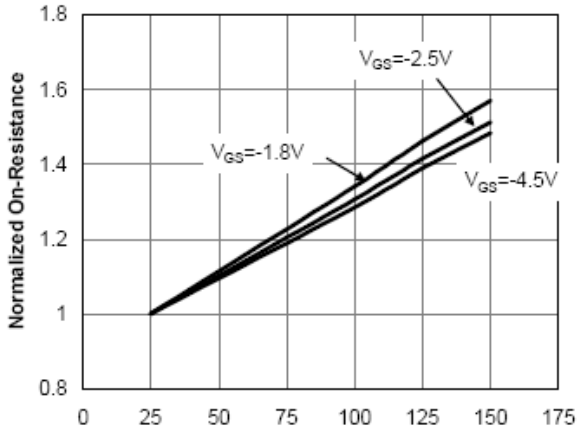


Figure 4: On-Resistance vs. Junction Temperature

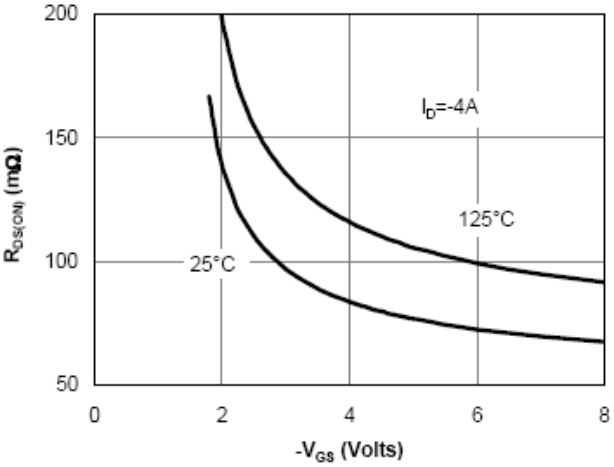


Figure 5: On-Resistance vs. Gate-Source Voltage

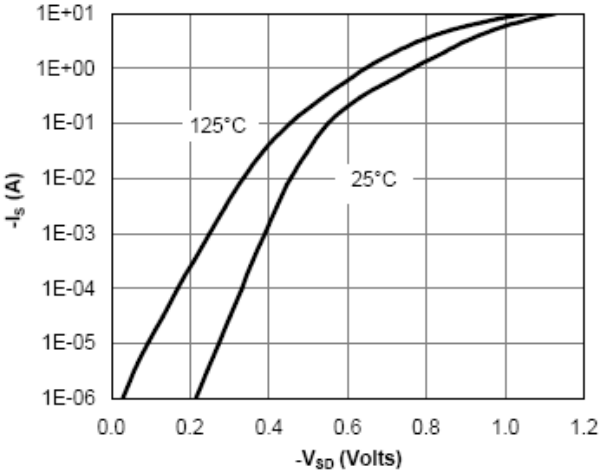


Figure 6: Body-Diode Characteristics

◆ TYPICAL CHARACTERICTICS

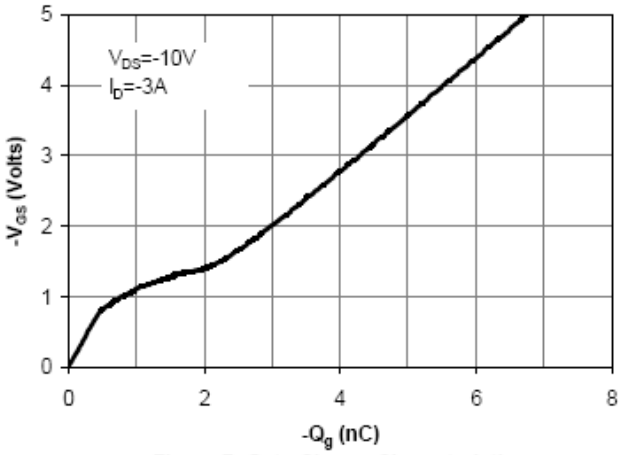


Figure 7: Gate-Charge Characteristics

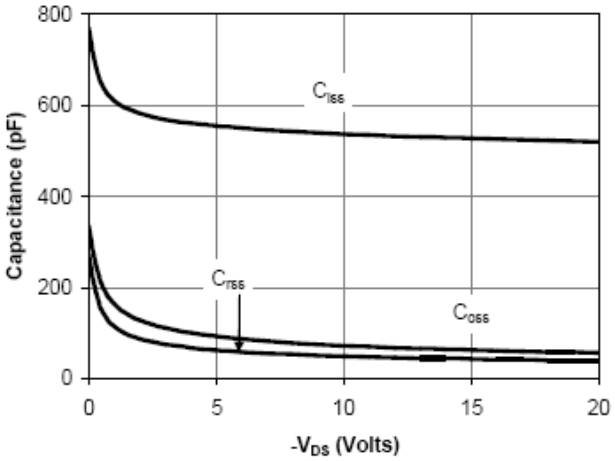


Figure 8: Capacitance Characteristics

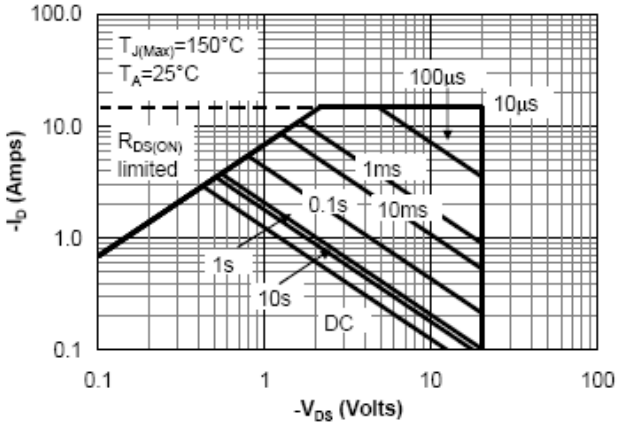


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

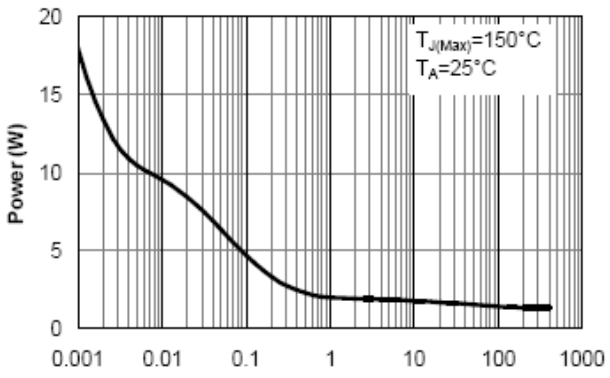


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

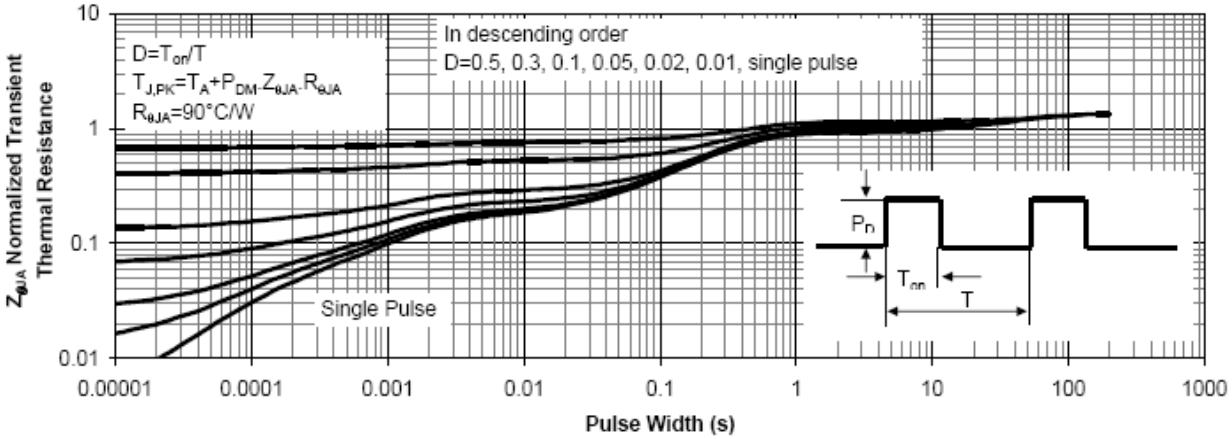
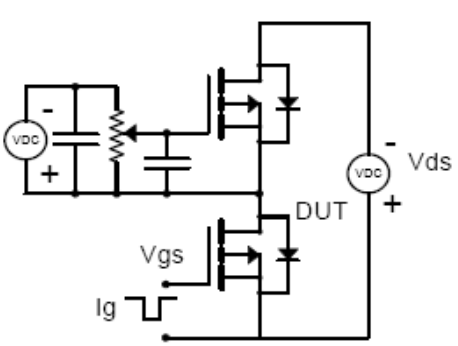
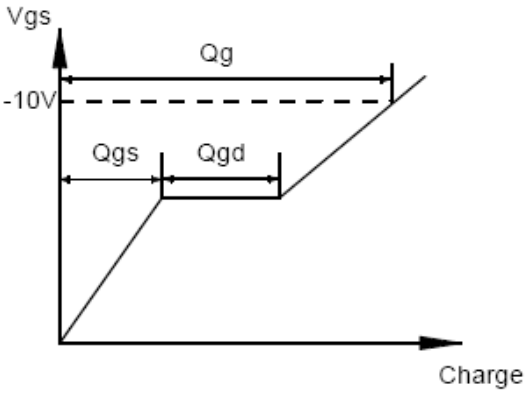


Figure 11: Normalized Maximum Transient Thermal Impedance

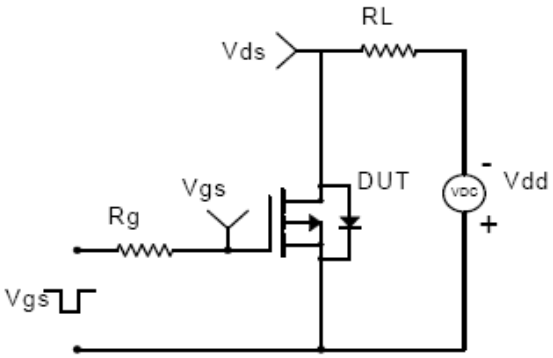
◆ TYPICAL CHARACTERICTICS

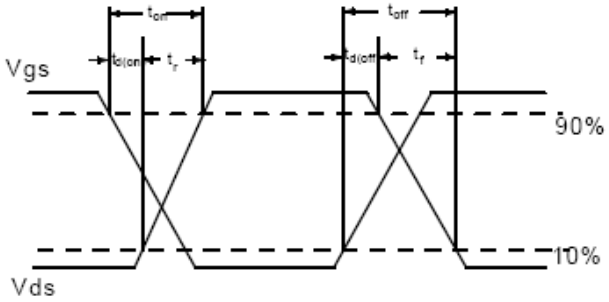
Gate Charge Test Circuit & Waveform



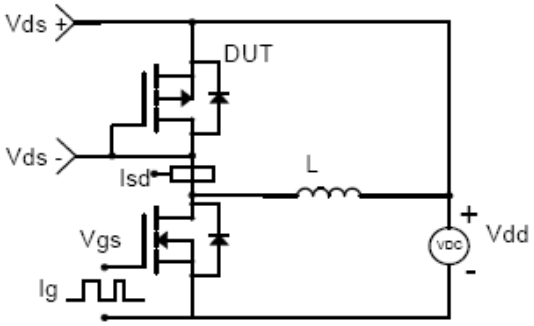


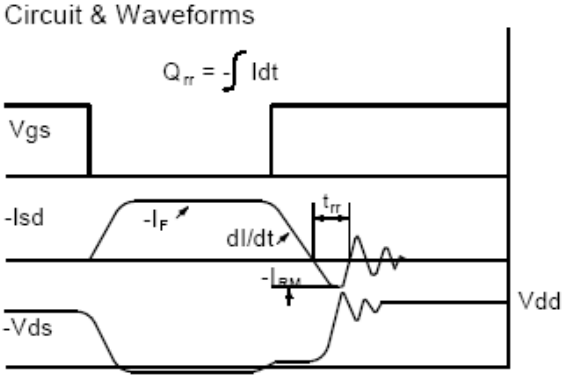
Resistive Switching Test Circuit & Waveforms





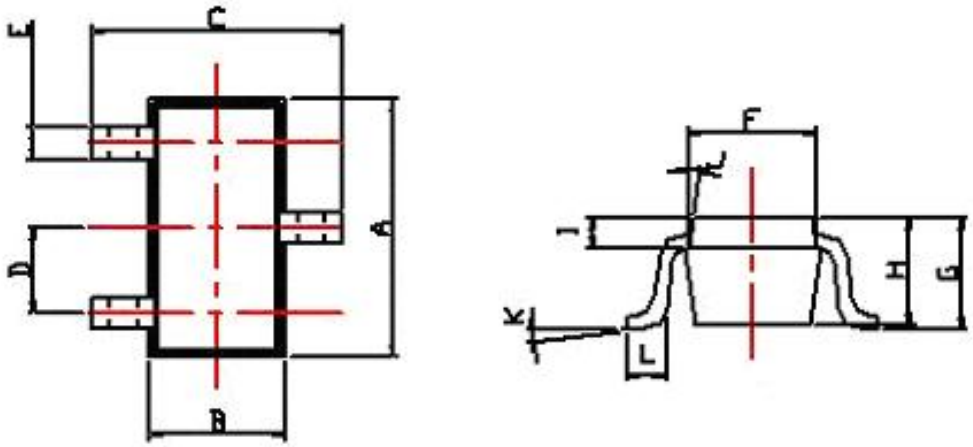
Diode Recovery Test Circuit & Waveforms





◆ PHYSICAL DIMENSIONS

3-Pin surface Mount SOT-23(S)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0.9	1.4
B	1.20	1.66	H	0.8	1.30
C	2.37	2.90	I	0.25	0.7
D	0.85	1.15	J	7 ± 2°.	
E	0.350 + 0.15/-0.05		K	0 ~ 10°.	
F	1.07	1.53	L	0.2 (MIN)	