

◆ DESCRIPTION

The MT2305 is the P-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other Battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

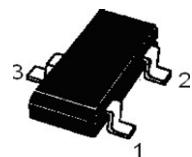
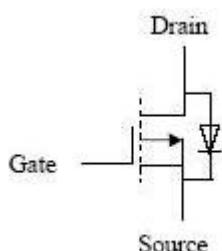
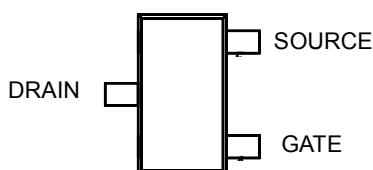
◆ FEATURES

- -30V/-2.6A, $R_{DS(ON)} = 130m\Omega$ @ $V_{GS} = -10V$
- -30V/-2.0A, $R_{DS(ON)} = 180m\Omega$ @ $V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

◆ APPLICATIONS

- POWER Management in Note
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC

◆ PIN CONFIGURATION



P- Channel Enhancement Mode MOSFET
◆ ABSOLUTE MAXIMUM RATINGS

($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Maximum	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $T_A = 25^\circ\text{C}$	I_D	-2.6	A
$T_A = 70^\circ\text{C}$		-2.0	
Pulsed Drain Current	I_{DM}	-10	A
Continuous Source Current (Diode Conduction)	I_S	-1.25	A
Power Dissipation $T_A = 25^\circ\text{C}$	P_D	1.25	W
$T_A = 70^\circ\text{C}$		0.8	
Operating junction temperature range	T_J	150	$^\circ\text{C}$
Storage temperature range	T_{STG}	- 55 to 150	$^\circ\text{C}$

◆ THERMAL RESISTANCE RATINGS

Thermal Resistance	Symbol	Maximum	Unit
Junction-to-Ambient	$R_{\theta JA}$	100	$^\circ\text{C/W}$

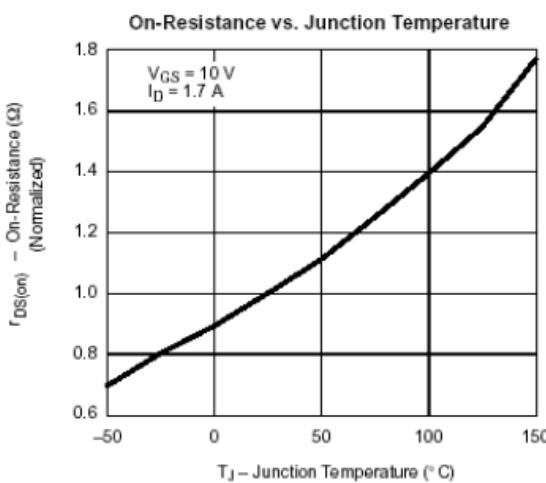
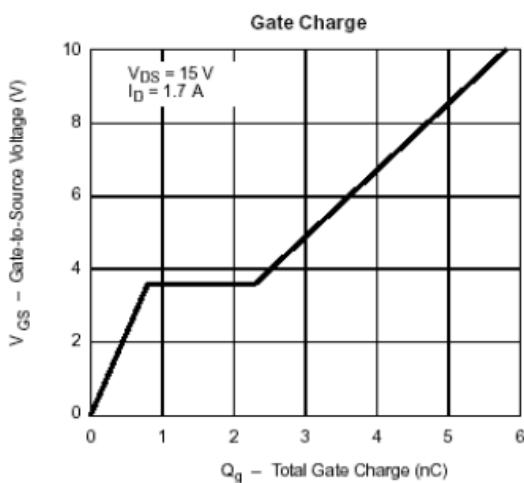
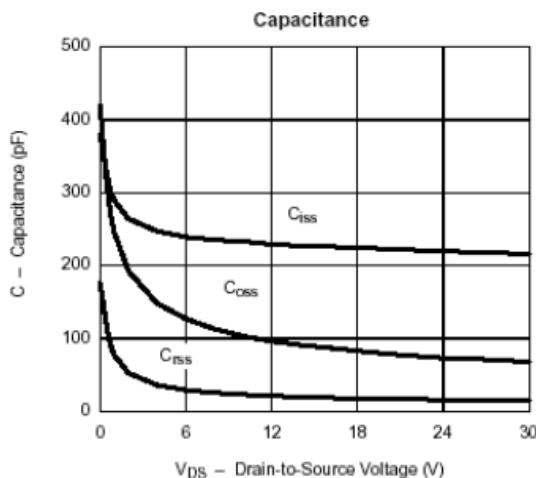
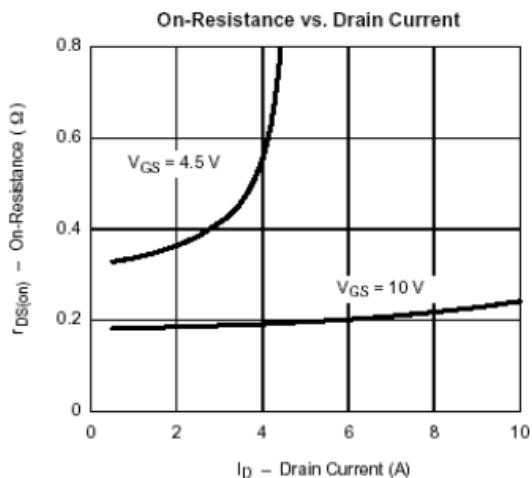
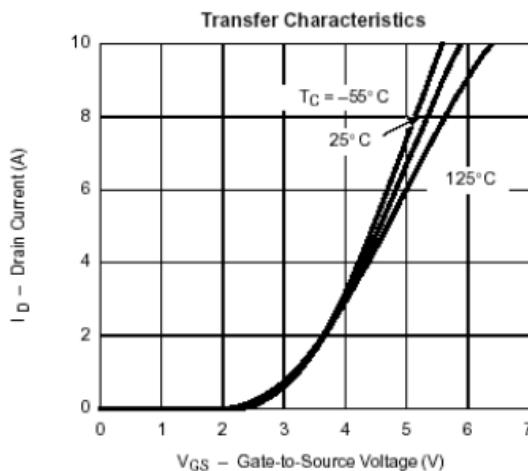
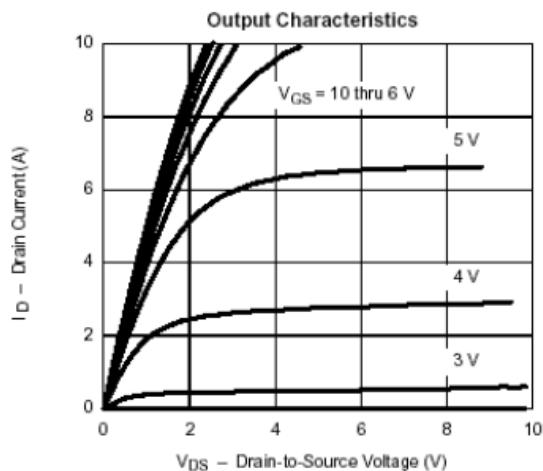
P- Channel Enhancement Mode MOSFET
◆ ELECTRICAL CHARACTERISTICS
 $(T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = -10\mu\text{A}$	-30	-	-	V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-1.0	-	-3.0	V
Gate Current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\text{V}, V_{GS} = 0\text{ V}$	-	-	-1	μA
		$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$	-	-	-10	
Forward Tran conductance	g_{fs}	$V_{DS} = -10\text{V}, I_D = -1.7\text{A}$	-	2.4	-	S
On-State Drain Current	$I_{D(\text{ON})}$	$V_{DS} \leq -5\text{V}, V_{GS} = -10\text{V}$	-6	-	-	A
Drain-Source On Resistance	$R_{DS(\text{ON})}$	$V_{GS} = -10\text{V}, I_D = -2.6\text{A}$	-	95	130	$\text{m}\Omega$
		$V_{GS} = -4.5\text{V}, I_D = -2.0\text{A}$	-	125	180	
Diode Forward Voltage	V_{SD}	$I_S = -1.25\text{A}, V_{GS} = 0\text{V}$	-	-0.8	-1.2	V
Dynamic Parameters						
Input Cap.	C_{iss}	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}, F = 1\text{MHz}$	-	226	-	pF
Output Cap.	C_{oss}		-	87	-	
Reverse Transfer Cap.	C_{rss}		-	19	-	
Total Gate Charge	Q_g	$V_{DS} = -15\text{V}, V_{GS} = -10\text{V}, I_D = -1.7\text{A}$	-	5.8	10	nC
Gate-Source Charge	Q_{gs}		-	0.8	-	
Gate-Drain Charge	Q_{gd}		-	1.5	-	
Turn-On Time	$t_{d(\text{ON})}$	$V_{DS} = -15\text{V}, R_L = 15\Omega, I_D = -1\text{A}, V_{GEN} = -10\text{V}, R_G = 6\Omega$	-	9	20	nS
	t_r		-	9	20	
Turn-Off Time	$T_{d(\text{OFF})}$		-	18	35	
	T_f		-	6	20	



P- Channel Enhancement Mode MOSFET

◆ TYPICAL CHARACTERISTICS

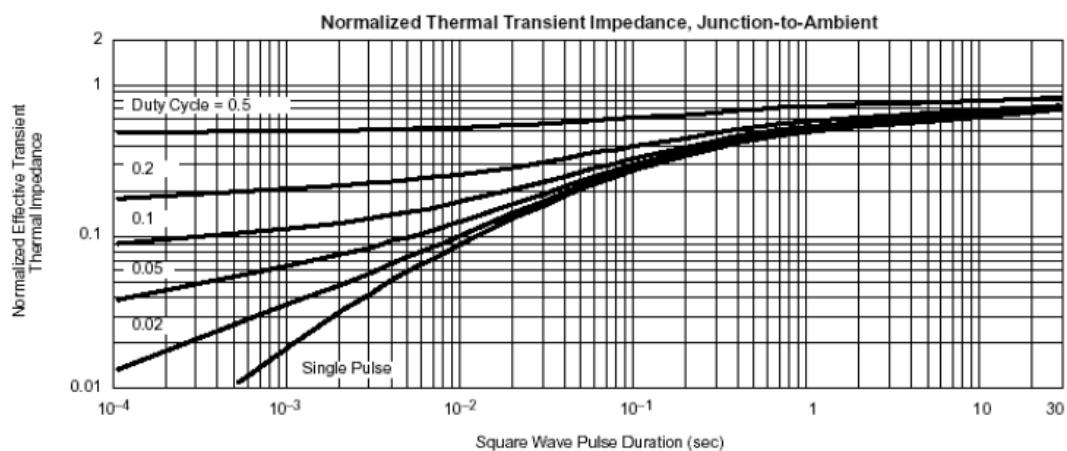
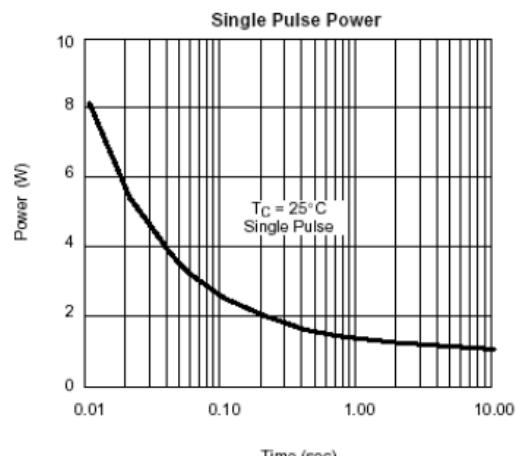
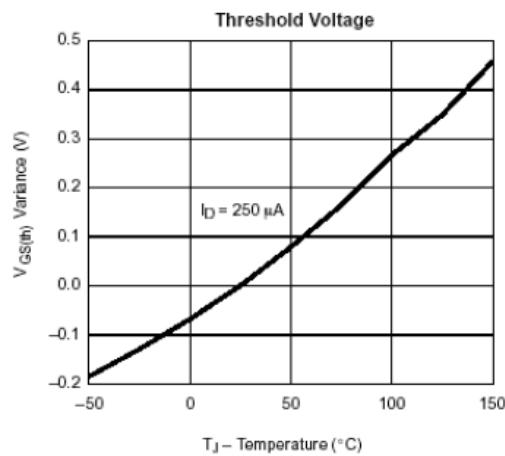
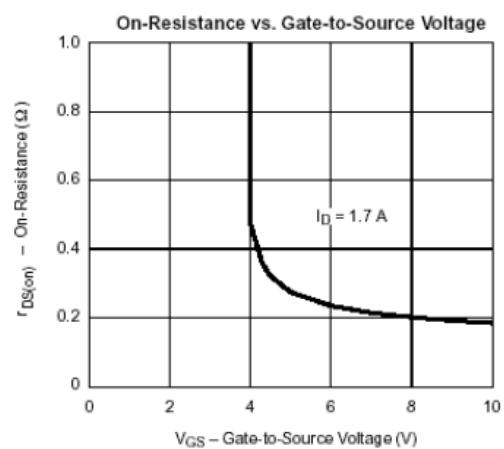
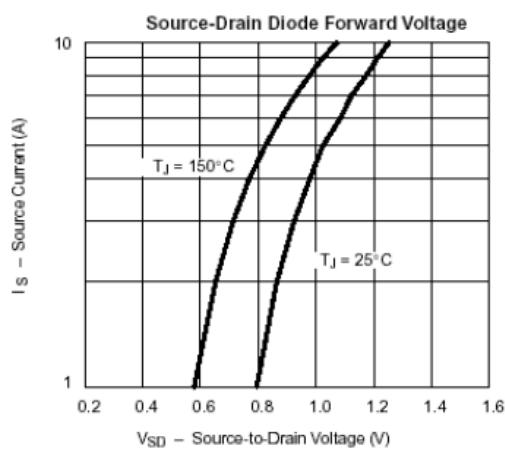
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P- Channel Enhancement Mode MOSFET

◆ TYPICAL CHARACTERISTICS

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**◆ PHYSICAL DIMENSIONS**

3-Pin surface Mount SOT-23

REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0.9	1.4
B	1.20	1.66	H	0.8	1.30
C	2.37	2.90	I	0.25	0.7
D	0.85	1.15	J	$7 \pm 2^\circ$.	
E	$0.350 + 0.15/-0.05$		K	$0 \sim 10^\circ$.	
F	1.07	1.53	L	0.2 (MIN)	