

**◆ DESCRIPTION**

The MT2304 is the N-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

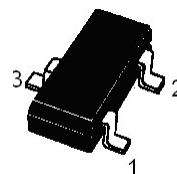
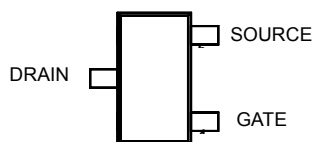
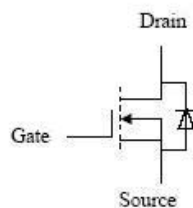
These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

**◆ FEATURES**

- 30V/3.2A,  $R_{DS(ON)} = 65m\Omega @ V_{GS} = 10V$
- 30V/2.0A,  $R_{DS(ON)} = 90m\Omega @ V_{GS} = 4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

**◆ APPLICATIONS**

- POWER Management in Note
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC

**◆ PIN CONFIGURATION**


**◆ ABSOLUTE MAXIMUM RATINGS**

 (T<sub>A</sub>=25°C Unless Otherwise Noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V <sub>DS</sub>	30	V
Gate-Source Voltage		V <sub>GS</sub>	±20	V
Continuous Drain Current	T <sub>A</sub> = 25°C	I <sub>D</sub>	3.2	A
	T <sub>A</sub> = 70°C		2.6	
Pulsed Drain Current		I <sub>DM</sub>	10	A
Continuous Source Current (Diode Conduction)		I <sub>S</sub>	1.25	A
Power Dissipation	T <sub>A</sub> = 25°C	P <sub>D</sub>	1.25	W
	T <sub>A</sub> = 70°C		0.8	
Operating junction temperature range		T <sub>J</sub>	150	°C
Storage temperature range		T <sub>STG</sub>	- 55 to 150	°C

**◆ THERMAL RESISTANCE RATINGS**

Thermal Resistance	Symbol	Maximum	Unit
Junction-to-Ambient	R <sub>θJA</sub>	100	°C/W

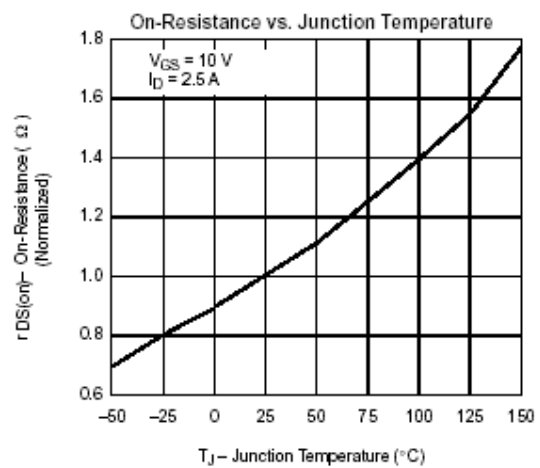
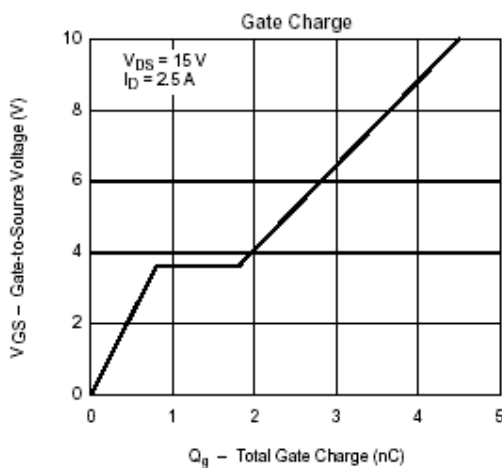
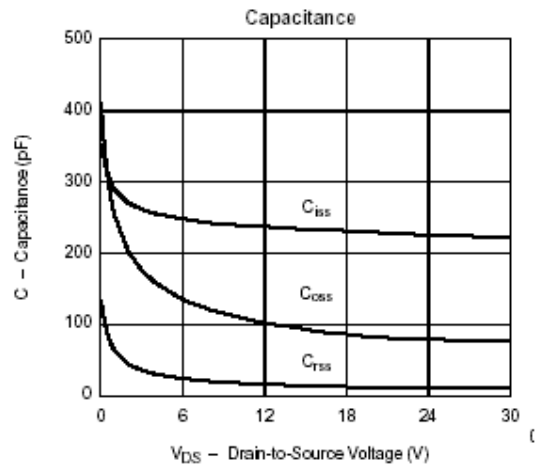
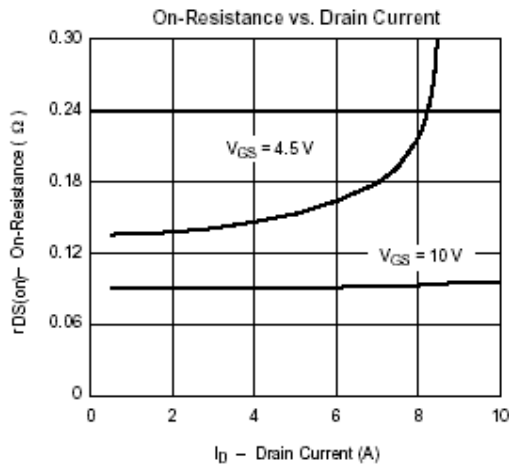
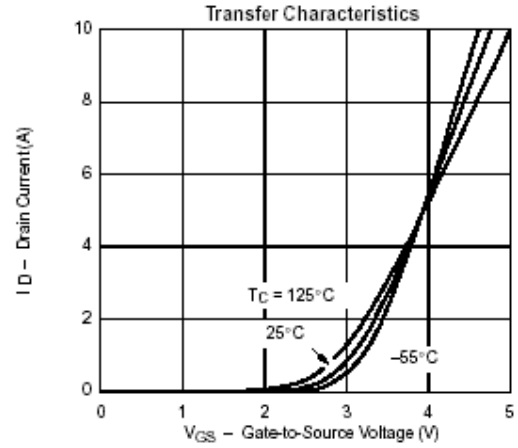
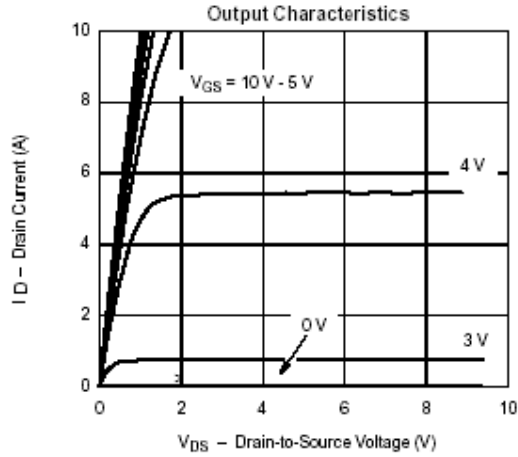
**◆ ELECTRICAL CHARACTERISTICS**

 (T<sub>A</sub>=25°C Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Parameters</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	30	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250μA	1.0	-	3.0	V
Gate Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 1.0 V	-	-	1	μA
		V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 55°C	-	-	10	
Forward Trans conductance	g <sub>fs</sub>	V <sub>DS</sub> = 4.5V, I <sub>D</sub> = 2.5A	-	4.6	-	S
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> ≥ 4.5V, V <sub>GS</sub> = 10V	6	-	-	A
		V <sub>DS</sub> ≥ 4.5V, V <sub>GS</sub> = 4.5V	4	-	-	
Drain-Source On Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 2.5A	-	50	65	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 2.0A	-	65	90	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 1.25A, V <sub>GS</sub> = 0V	-	0.82	1.2	V
<b>Dynamic Parameters</b>						
Input Cap.	C <sub>iss</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V, F = 1MHz	-	240	-	pF
Output Cap.	C <sub>oss</sub>		-	110	-	
Reverse Transfer Cap.	C <sub>rss</sub>		-	17	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 2.5A	-	4.5	10	nC
Gate-Source Charge	Q <sub>gs</sub>		-	0.8	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	1.0	-	
Turn-On Time	T <sub>D(ON)</sub>	V <sub>DD</sub> = 15V, R <sub>L</sub> = 15Ω, I <sub>D</sub> = 1A, V <sub>GEN</sub> = 10V, R <sub>G</sub> = 6Ω	-	8	20	nS
	t <sub>r</sub>		-	12	30	
Turn-Off Time	T <sub>D(OFF)</sub>		-	17	35	
	t <sub>f</sub>		-	8	20	

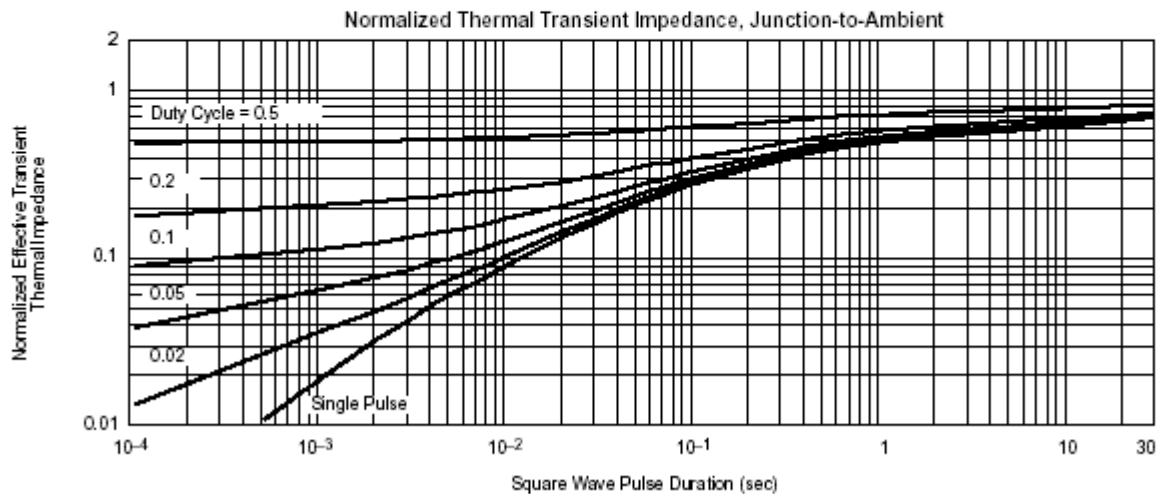
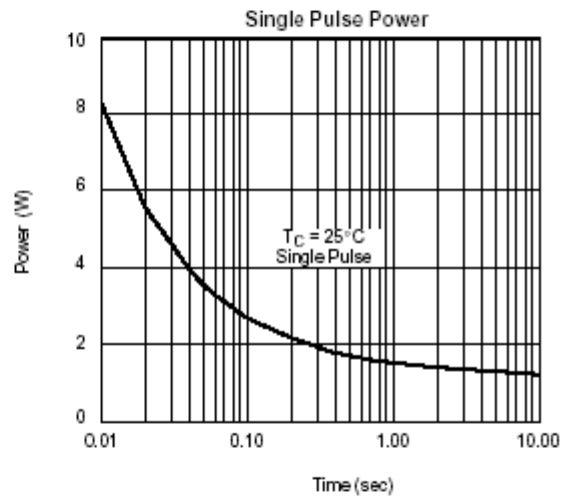
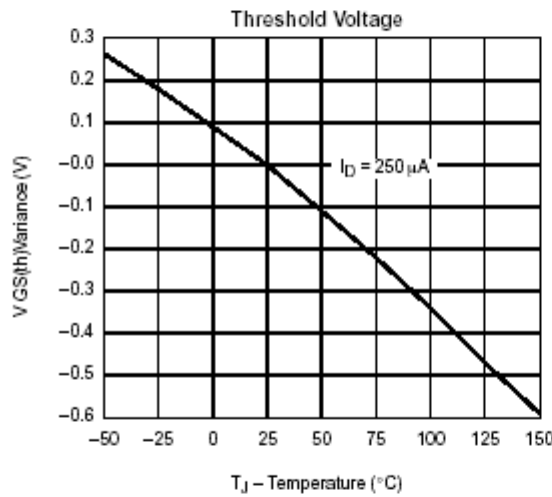
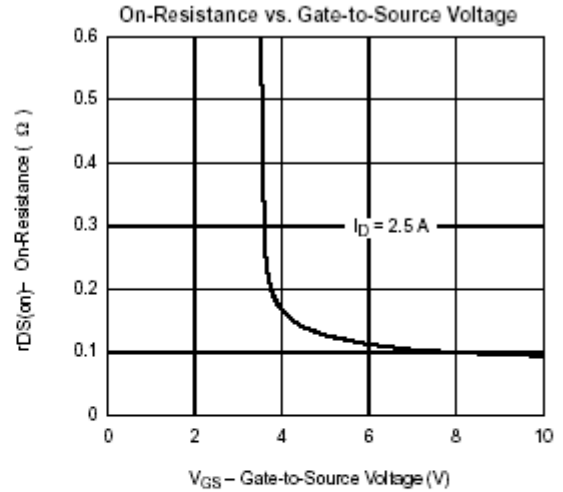
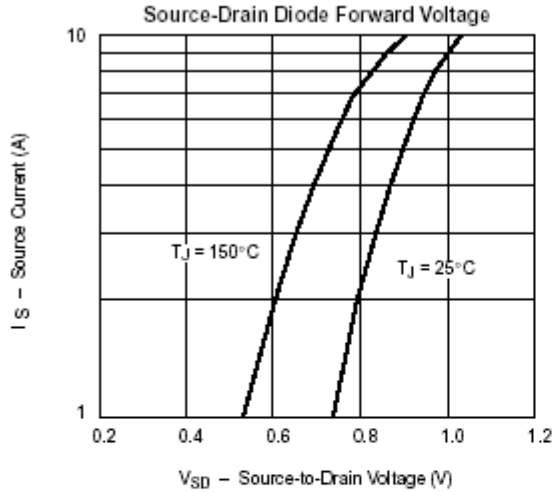
**◆ TYPICAL CHARACTERISTICS**

(25°C Unless Noted)



**◆ TYPICAL CHARACTERISTICS**

(25°C Unless Noted)



**◆ PHYSICAL DIMENSIONS**
**3-Pin surface Mount SOT-23**
