

P- Channel Enhancement Mode MOSFET
◆ DESCRIPTION

The MT4435 MOSFET from MATRIX provide the designer with the best combination of fast switching, Buggerized device design, low on-resistance and cost-effectiveness.

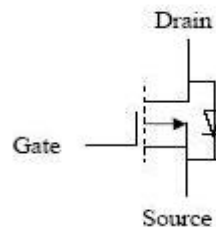
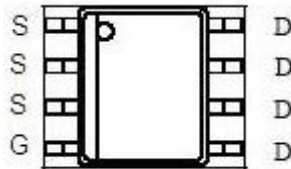
The SO-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

◆ FEATURES

- -30V/-8A, $R_{DS(ON)} = 20m\Omega @ V_{GS} = -10V$
- SO-8 package design
- Simple Drive Requirement
- Low On-resistance
- Fast Switching

◆ APPLICATIONS

- POWER Management in Note
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

◆ PIN CONFIGURATION

◆ ABSOLUTE MAXIMUM RATINGS

($T_A=25^\circ C$ Unless Otherwise Noted)

Parameter	Symbol	Maximum	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ³	I_D	$T_A=25^\circ C$	-8
		$T_A=70^\circ C$	-6
Pulsed Drain Current ^{1,2}	I_{DM}	-50	A
Total Power Dissipation	P_D	2.5	W
Linear Derating Factor		0.02	W/ $^\circ C$
Storage Temperature Range	T_{STG}	-55 to 150	$^\circ C$
Operating Junction Temperature Range	T_J	- 55 to 150	$^\circ C$

P- Channel Enhancement Mode MOSFET
◆ THERMAL RESISTANCE RATINGS

Thermal Resistance	Symbol	Maximum	Unit
Thermal Resistance Junction-ambient	R_{thj-a}	50	$^{\circ}\text{C}/\text{W}$

◆ ELECTRICAL CHARACTERISTICS

 ($T_A=25^{\circ}\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Parameters						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$	-30	-	-	V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_j$	Reference to $25^{\circ}\text{C}, I_D = -1\text{mA}$	-	-0.04	-	$\text{V}/^{\circ}\text{C}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS} = -10\text{V}, I_D = -8\text{A}$	-	15	20	m Ω
		$V_{GS} = -4.5\text{V}, I_D = -5\text{A}$	-	26	32	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	-1	-	-3	V
Forward Transconductance	g_{fs}	$V_{DS} = -15\text{V}, I_D = -8\text{A}$	-	20	-	S
Drain-Source Leakage Current	I_{DSS}	$T_J=25^{\circ}\text{C}$ $V_{DS} = -30\text{V}, V_{GS} = 0\text{V}$	-	-	-1	uA
		$T_J=70^{\circ}\text{C}$ $V_{DS} = -24\text{V}, V_{GS} = 0\text{V}$	-	-	-25	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
Dynamic Parameters						
Total Gate Charge ²	Q_g	$I_D = -4.6\text{A}, V_{DS} = -15\text{V}, V_{GS} = -10\text{V}$	-	36	-	nC
Gate-Source Charge	Q_{gs}		-	5.5	-	
Gate-Drain("Miller")Charge	Q_{gd}		-	3.5	-	
Turn-on Delay Time ²	$t_{d(on)}$	$V_{DS} = -15\text{V}, I_D = -1\text{A}, R_G = 6\Omega, V_{GS} = -10\text{V}, R_D = 15\Omega$	-	12	-	ns
Rise Time	t_r		-	8	-	
Turn-off Delay Time	$T_{d(off)}$		-	75	-	
Fall time	T_f		-	40	-	
Input Capacitance	C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = -15\text{V}, f = 1.0\text{MHz}$	-	1530	-	pF
Output Capacitance	C_{oss}		-	900	-	
Reverse Transfer Capacitance	C_{rss}		-	280	-	
Gate Resistance	R_g	$F = 1.0\text{MHz}$	-	6	9	Ω

P- Channel Enhancement Mode MOSFET
◆ Source-Drain Diode

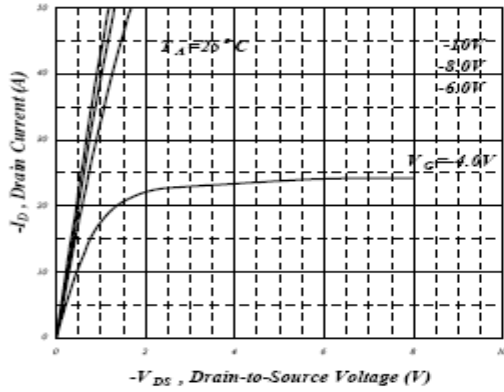
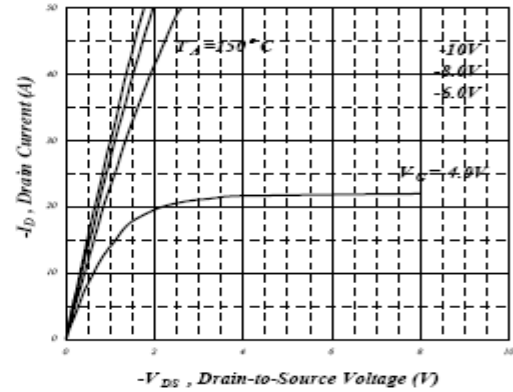
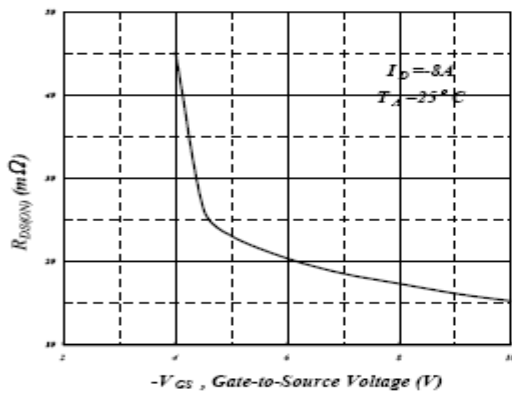
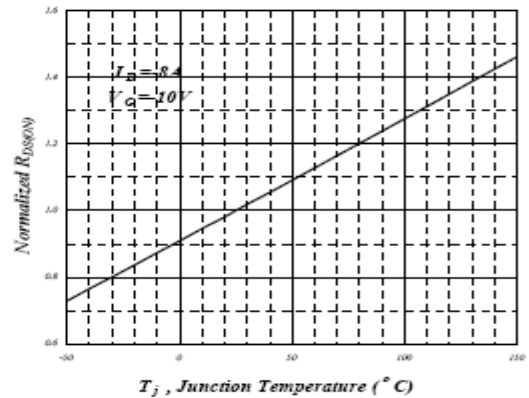
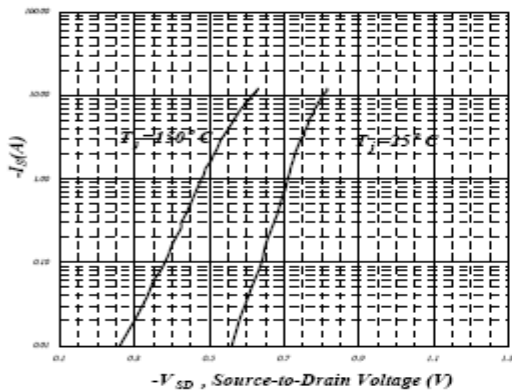
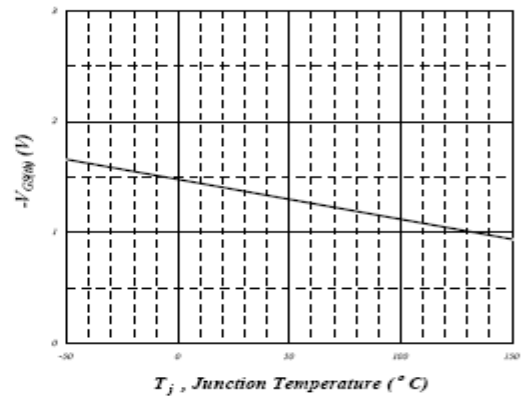
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Forward On Voltage ²	V_{SD}	$I_S = -2.1A, V_{GS} = 0V$	-	-	-1.2	V
Reverse Recovery Time ²	t_{rr}	$I_S = -5A, V_{GS} = 0V,$	-	55	-	ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/us$	-	83	-	nc

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse width $\leq 300us$, duty cycle $\leq 2\%$
3. Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10sec$; 125°CW when mounted on Min.copper pad.

P- Channel Enhancement Mode MOSFET
◆ TYPICAL CHARACTERISTICS

(25°C Unless Noted)


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. On-Resistance v.s. Gate Voltage

Fig 4. Normalized On-Resistance v.s. Junction Temperature

Fig 5. Forward Characteristic of Reverse Diode

Fig 6. Gate Threshold Voltage v.s. Junction Temperature

P- Channel Enhancement Mode MOSFET

◆ TYPICAL CHARACTERISTICS

(25°C Unless Noted)

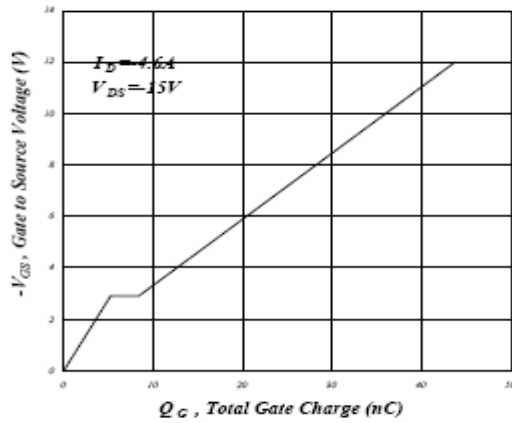


Fig 7. Gate Charge Characteristics

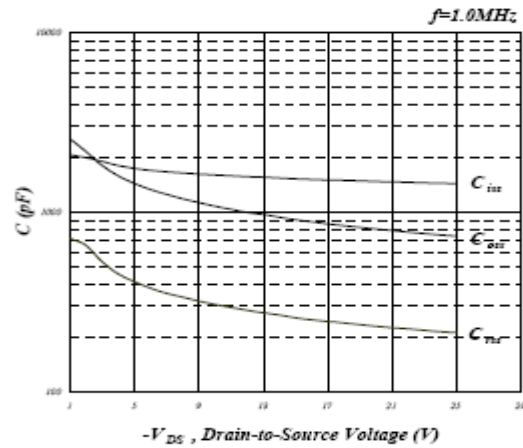


Fig 8. Typical Capacitance Characteristics

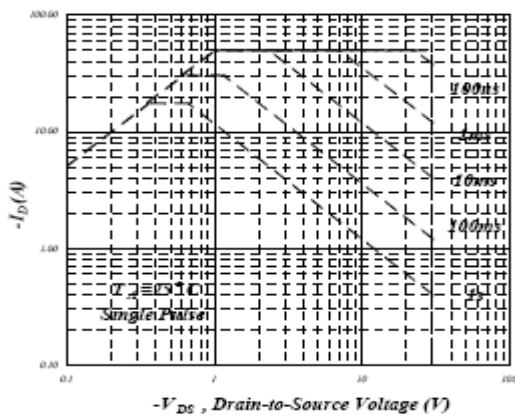


Fig 9. Maximum Safe Operating Area

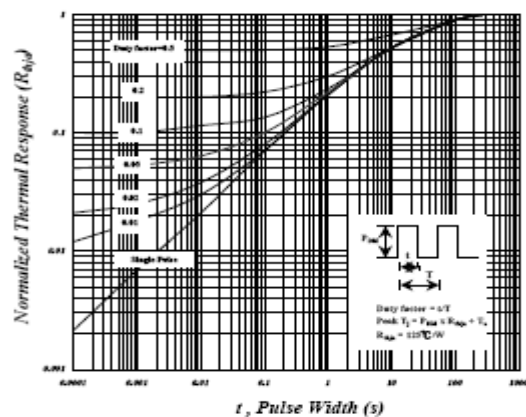


Fig 10. Effective Transient Thermal Impedance

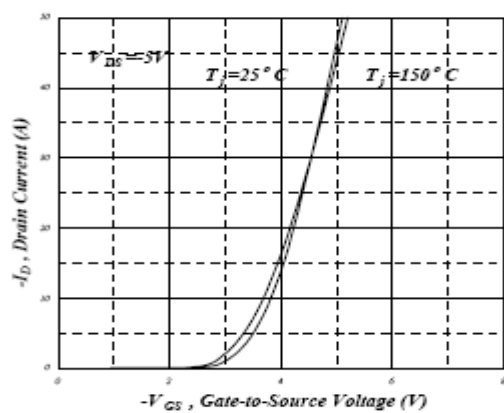


Fig 11. Transfer Characteristics

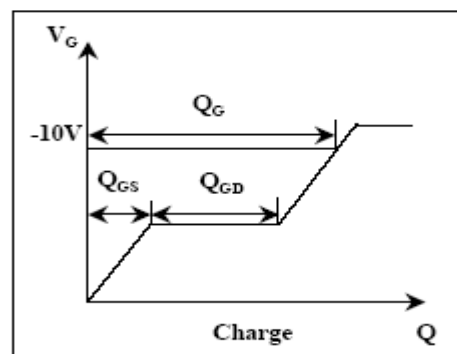


Fig 12. Gate Charge Circuit

P- Channel Enhancement Mode MOSFET
◆ PHYSICAL DIMENSIONS:
8-Pin Plastic S.O.I.C. (M)
