**2A Sink/Source Bus Termination Regulator**

## ◆ DESCRIPTION

The MT9174 is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the JEDEC SSTL_2 and SSTL_18 or other specific interfaces such as HSTL, SCSI-2 and SCSI-3 etc. devices requirements.

The regulator is capable of actively sinking or sourcing up to 2A while regulating an output voltage to within 40mV. The output termination voltage cab be tightly regulated to track 1/2 VDDQ by two external voltage divider resistors or the desired output voltage can be pro-grammed by externally forcing the REFEN pin voltage.

The MT9174 also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shut-down protection.

## ◆ FEATURES

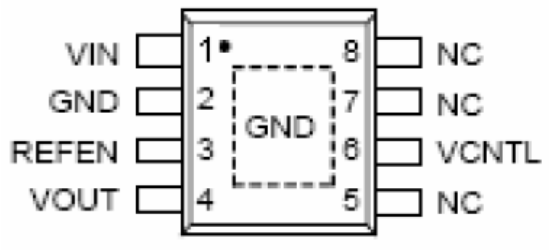
- Ideal for DDR-I, DDR-II and DDR-III $V_{TT}$ Applications
- Sink and Source 2A Continuous Current
- Integrated Power MOSFETs
- Generates Termination Voltage for SSTL_2, SSTL _18, HSTL, SCSI-2 and SCSI-3 Interfaces.
- High Accuracy Output Voltage at Full-Load
- Output Adjustment by Two External Resistors
- Low External Component Count
- Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output
- Current Limiting Protection
- On-Chip Thermal Protection
- Available in PSOP-8 (Exposed Pad) Packages
- VIN and VCNTL No Power Sequence Issue
- RoHS Compliant and 100% Lead (Pb)-Free

## ◆ APPLICATIONS

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses
- DDR-I, DDR-II and DDR-III Memory Systems

## ◆ PIN CONFIGURATIONS

**PSOP-8** (Top View)




**MT9174P**

## ◆ ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Parameter | Maximum | Unit |
|---|---|---|---|
| Input Voltage | $V_{IN}$ | 6 | V |
| Control Voltage | $V_{CNTL}$ | 6 | V |
| Power Dissipation | $P_D$ | Internally Limited | - |
| ESD Rating | - | 3 | KV |
| Storage Temperature Range | $T_S$ | -65 to 150 | ℃ |
| Lead Temperature (Soldering, 5 sec.) | $T_{LEAD}$ | 260 | ℃ |
| Package Themal Resistance | $\theta_{JC}$ | 28 | ℃/W |

## ◆ OPERATING RATING(2)

| Symbol | Parameter | Maximum | Unit |
|---|---|---|---|
| Input Voltage | $V_{IN}$ | 2.5 to 1.5 ± 3% | V |
| Control Voltage | $V_{CNTL}$ | 5.5 or 3.3 ± 5% | V |
| Ambient Temperature | $T_A$ | -40 to + 85 | ℃ |
| Junction Temperature | $T_J$ | -40 to + 125 | ℃ |

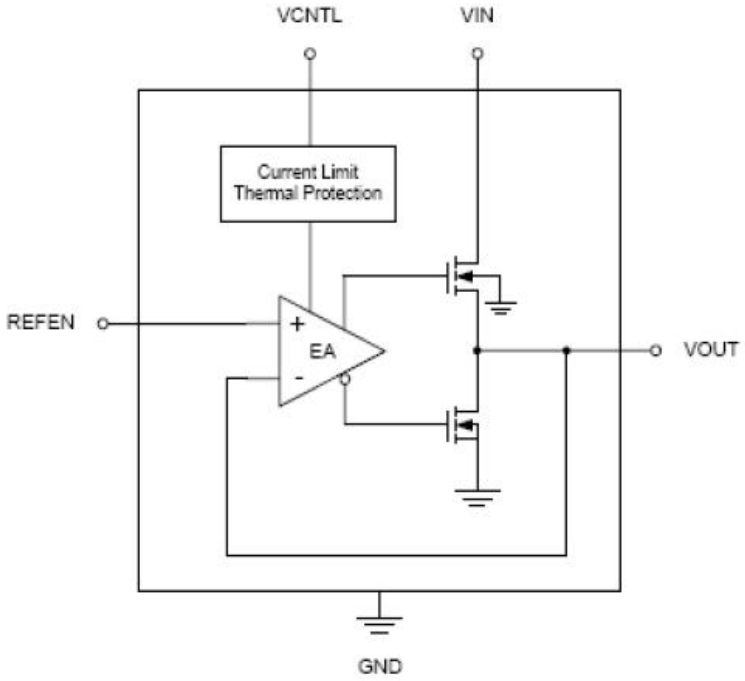
## ◆ ORDERING INFORMATION

| Device | Package | | $T_A$ (°C) |
|---|---|---|---|
| MT9174P | P | PSOP-8 | -40 to 85 |

## ◆ PIN DESCRIPTION

| No. | MT9174 PIN Name | Function |
|---|---|---|
| 1 | VIN | Power Input |
| 2 | GND | Ground |
| 3 | REFEN | Reference Voltage input and Chip Enable |
| 4 | $V_{OUT}$ | Output Voltage |
| 5 | NC | No Connection |
| 6 | NC | No Connection |
| 7 | $V_{CNTL}$ | Gate Drive Voltage |
| 8 | NC | No Connection |

## ◆ BLOCK DIAGRAM



## ◆ ELECTRICAL CHARACTERISTICS

$V_{IN}$=2.5V/1.8V/1.5V, $V_{CNTL}$=3.3V, $V_{REFEN}$=1.25V/0.9V/0.75V, $C_{OUT}$=10μF (Ceramic), $T_A$=25ºC, unless otherwise specified

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| $V_{CNTL}$ Operation Current | $I_{CNTL}$ | $I_{OUT}$=0A | - | 1 | 2.5 | mA |
| Standby Current | $I_{STBY}$ | $V_{REFEN}$<0.2V(Shutdown),$R_{LOAD}$=180Ω | - | 50 | 90 | uA |
| **Output (DDR / DDR II / DDR III)** | | | | | | |
| Output Offset Voltage(3) | $V_{OS}$ | $I_{OUT}$ = 0A | -20 | - | +20 | mV |
| Load Regulation(4) | $\Delta V_{LOAD}$ | $I_{OUT}$ =+2A | -20 | - | +20 | mV |
| | | $I_{OUT}$ = -2A | | | | |
| **Protection** | | | | | | |
| Current limit | $I_{LIM}$ | | 2.2 | - | - | A |
| Thermal Shutdown Temperature | $T_{SD}$ | 3.3V ≤ $V_{CNTL}$ ≤ 5V | 125 | 170 | - | ℃ |
| Thermal Shutdown Hysteresis | $\Delta T_{SD}$ | 3.3V ≤ $V_{CNTL}$ ≤ 5V | - | 35 | - | ℃ |
| **REFEN Shutdown** | | | | | | |
| Shutdown Threshold | $V_{IH}$ | Enable | 0.6 | - | - | V |
| | $V_{IL}$ | Shutdown | - | - | 0.2 | V |

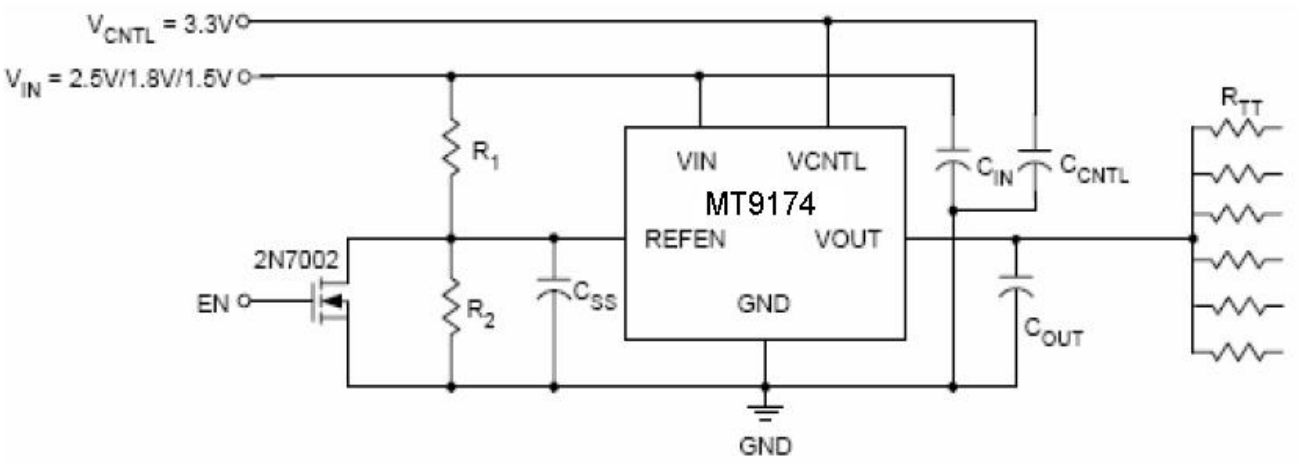
Note 1: Exceeding the absolute maximum rating may damage the device.

Note 2: $V_{OS}$ offset is the voltage measurement defined as $V_{OUT}$ subtracted from $V_{REFEN}$

Note 3: $V_{OS}$ offset is the voltage measurement defined as $V_{OUT}$ subtracted from $V_{REFEN}$.

Note 4: Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 2A.

## ◆ Application Diagram




$R_1 = R_2 = 100K\Omega$, $R_{TT} = 50\Omega/33\Omega/25\Omega$

$C_{OUT}$, min = 10μF (Ceramic) + 1000μF under the worst case testing condition

$C_{SS}$ = 1μF, $C_{IN}$ = 470μF(Low ESR), $C_{CNTL}$ = 47μF

## ◆ Application Information

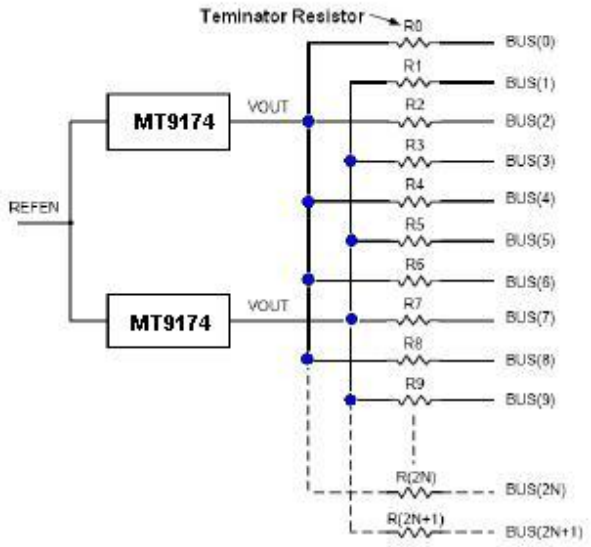
**Input Capacitor and Layout Consideration**

Place the input bypass capacitor as close as possible to the MT9174. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance. Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between MT9174 and the preceding power converter.

**Consideration while designs the resistance of voltage divider**

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on $V_{REFEN}$ is below 0.2V.In addition, the capacitor and voltage divider form the lowpass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.

## ◆ Application Information( continued )




**Thermal Consideration**

MT9174 regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continued operation, do not exceed maximum operation junction temperature 125℃. The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = ( T_{J(MAX)} - T_A ) / \Theta_{JA}$$

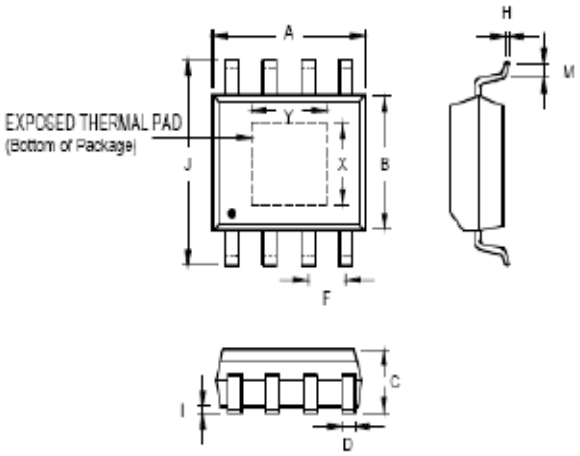
Where $T_{J(MAX)}$ is the maximum operation junction temperature 125℃, $T_A$ is the ambient temperature and the $\Theta_{JA}$ is the junction to ambient thermal resistance. The junction to ambient thermal resistance ($\Theta_{JA}$ is layout dependent) for PSOP-8 package (Exposed Pad) is 75℃/W on standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The maximum power dissipation at $T_A$ = 25℃ can be calculated by following formula:

$$P_{D(MAX)} = (125℃ - 25℃) / 75℃/W = 1.33W$$

The thermal resistance $\Theta_{JA}$ of PSOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the expose pad of PSOP-8 package. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow.

## ◆ PHYSICAL DIMENSIONS:

**8-Pin Plastic S.O.I.C. (P)**




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 4.801 | 5.004 | 0.189 | 0.197 |
| B | 3.810 | 3.988 | 0.150 | 0.157 |
| C | 1.346 | 1.753 | 0.053 | 0.069 |
| D | 0.330 | 0.508 | 0.013 | 0.020 |
| F | 1.194 | 1.346 | 0.047 | 0.053 |
| H | 0.191 | 0.254 | 0.008 | 0.010 |
| I | 0.000 | 0.152 | 0.000 | 0.006 |
| J | 5.791 | 6.198 | 0.228 | 0.244 |
| M | 0.406 | 1.270 | 0.016 | 0.050 |
| X | 2.057 | 2.515 | 0.081 | 0.099 |
| Y | 2.057 | 3.404 | 0.081 | 0.134 |